User Description

Integrated Circuit for Electrically Conditioning the Optical Signal When Transmitting Data by Means of Fiber-Optic Cables

(M4A3-64/32-12VI)

Version: 0.5

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Liability Exclusion

Although we have tested the contents of this document regarding agreement with the described hardware and software, deviations cannot be ruled out, and complete agreement cannot be guaranteed. However, the data in this document is checked periodically. Necessary corrections are included in subsequent versions. We gratefully accept suggestions for improvement.

Subject to technical changes

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1. General

The integrated circuit for conditioning the optical signal is an interface circuit for **connecting a station** on the fiber-optic (FO) bus, for **retiming** (= compensating for signal distortions) and **repeating** (= message frame routing) DP message frames on PROFIBUS DP/FO.

Areas of Application:
- Slaves in an open line structure
- Masters in an open line structure

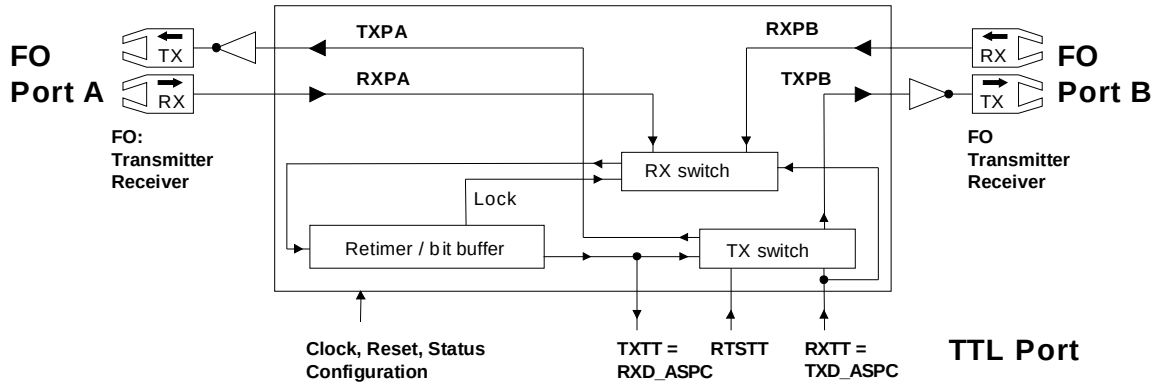
In addition to the integrated circuit for conditioning the optical signal, fiber-optic components (transmitter/receiver) and external send drivers are needed.

Message frames are not evaluated in the circuit for conditioning the optical signal. The chip provides a TTL interface to connect a DP ASIC for the actual evaluation/processing of the message frames.

An RS 485 transceiver can (with restrictions) be connected to the MPI - Auxiliary Interface. Copper segments are not to be connected here! The cable distortions on the RS 485 interface must not exceed +/- 20 ns. This application is intended for connecting a module with a copper interface to the fiber-optic bus. Here, only a short point-to-point connection terminated on both ends is to be used.

The integrated circuit is implemented with a 44-pin chip in TQPF casing and reduced power loss. The complete and operational chip can be ordered from Siemens AG (Automation & Drives) under the numbers 6ES7 **195-0EA00-0XA0** - 10 Pieces and **6ES7 195-0EA10-0XA0** - 160 Pieces.

2. Block Diagram



Signal Ports/Chip Segments	Function
FO Port A	**Line:** fiber-optic connection duplex line "A" (Port A/B = symmetrical)
FO Port B	**Line:** fiber-optic connection duplex line "B" (Port A/B = symmetrical)
TTL Port (RXD, TXD, RTS)	TTL side; direct connection to a PROFIBUS ASIC (TTL) Connection to an RS 485 driver (reti == high)
Clock/Reset/Status/Configuration	Auxiliary signals
RX switch (lock)	Prioritizes the receive signals and selects a preferred direction. The switch switches the RX signal to the retimer/bit buffer for further processing.
Retimer/Bit buffer	The input signal is scanned and distortions are corrected. A bit buffer FIFO compensates for clock drifts from the external transmitter and the chip for conditioning the signal. The corrected signal is routed to the TX switch.
TX switch	Depending on the prioritized preferred direction, the signal flow is routed to the FOSCI (fiber-optic cable coupler) ports.

This chip is a three-gate chip that connects three bidirectional ports with each other. These are the FO ports A and B, and the TTL port.

During an idle phase (message frame interval), the RX switch monitors the Receive lines of all three ports. If an RX_Port becomes active, it is prioritized. The Receive mode of the remaining ports is switched off.

The received signal is conditioned in the retimer/bit buffer, and buffered.

The transmission switch accepts the data from the bit buffer and routes it to the transmission outputs according to the following transfer scheme.

Received from Interface ...			**Routing to Interface ...**		
RX_ Port_A	high	high	high	TX_Port_B	TX_TTL
high	RX_Port_B	high	TX_Port_A	high	TX_TTL
high	high	RX_TTL	TX_Port_A	TX_Port_B	ECHO 1:1

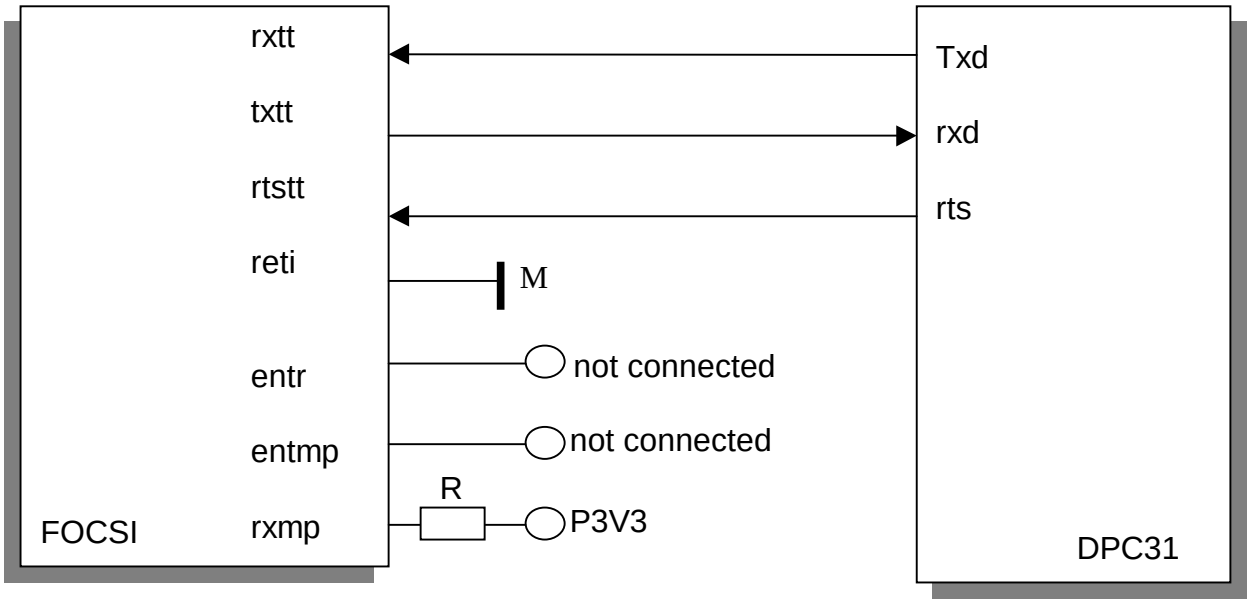
There is a time delay between the received signal and the transmitted signal due to the scanning process and the buffer.

At TXTT, the signals received at the TTL port (RXTT) are mirrored to the source. Some DP ASICs expect this echo function. The echo function is NOT time-delayed (that is, except for gate runtimes identical with RXTT).

An RS 485 transceiver can be connected to the TTL port.
Attention: It is not possible to build an optical ring with that device. Only a bus line is possible

3. Application Example: Chip for Conditioning the Optical Signal in Connection with a DP_ASIC

Interface to DP-ASIC (with transmission control)



The Interface to the DP-ASIC with RTS – transmission control is the recommended standard interface of the FOCSI. Due to the early timing of the RTS signal compared with TXD on the side of the FOCSI – TTL Side no retimer is necessary. reti = low switches off the retimer.

4. Parts List

Chip for conditioning the optical signal	**6ES7 195-0EA00-0XA0** **6ES7 195-0EA10-0XA0**	Siemens
Transmitter	QFBR T507	Hewlett Packard
Receiver	QFBR R507	Hewlett Packard

Note:
Fiber-optic receivers/transmitters are components of the HP series 508.

Function	Standard Device 10 Mbits	Selected Device 12 Mbits
Transmitter	HFBR-1528	QFBR-T507
Receiver	HFBR-2528	QFBR-R507

Note:
The pair receiver/sender must be latched prior to soldering.

5. Literature on the Internet

Hewlett-Packard

http://www.hp.com — Homepage HP Components
http://www.agilent.com — Internet address of Agilent Technologies:

6. Fiber-Optic Components

POF Fiber-Optic Cable

see: Catalog Siemens IK 10, pages 10,11

CUPOFLEX Simplex Core, unassembled — 5DX6 312-4AA01
CUPOFLEX Duplex Core, unassembled — 5DX6 322-4AA01

7. Configuration

Port	Function/Application
RETI	This control port is wired statically. It specifies whether the signal RXTT is switched by means of the "detour" retimer, or directly to the TX switch.
RETI = lo	If the ASPC2/SPC3 ASIC is coupled directly (TTL signals) with the chip for conditioning the optical signal, the send signal TX_ASIC == RXTT is not significantly distorted, and does not have to be "retimed" for that reason. Note: RTS must be wired. If RETI=lo, the RX switch has no lead time for prioritizing the receive port. This must be done with RTS which the ASIC activates shortly before it transmits.
RETI = hi	The signal received at RXTT is processed by means of the retimer. This is a must if an RS 485 transceiver is connected at the chip for conditioning the optical signal. This also applies if the RTS is applied to the RS 485 interface.
RTSTT	High active input. Send request by the ASIC to the chip for conditioning the optical signal. Is evaluated by the receive port prioritization (>> a floating input blocks the FOSCI (fiber-optic cable coupler) because it is interpreted as a continuous request).

8. µP Interface

These signals remain "reserved“.

9. Chip Handling

TQPF casings must be dried prior to soldering.

10. Application Notes

QFBR R507: Filtering the VCC of the fiber-optic receiver as described in the HP data sheet must be adhered to. The backup capacitor must be located in the immediate vicinity of the receiver.
(Error: the receiver may start oscillating through its input noise, even without light incidence. Viewed on an oscilloscope, this interference can only be distinguished with difficulty from a 12-Mbps message frame. The interference blocks the chip for conditioning the optical signal and creates "data scrap" in the entire fiber-optic network.)

QFBR R507: The casing material of the receiver is electrically conductive. The wire link must be placed on GND or shield.

QFBR R507, mechanical destruction: In one case, the receiver was destroyed through a POF fiber-optic cable. The error was a sporadic receive interruption, depending on the mechanical load on the chip. Cause: In a fiber-optic connector that was pressed together poorly, the light conducting core was movable in the connector and protruded under pressure up to 1.5 mm.

Clock 48 MHz: The clock does not have to be in-phase or identical with the operating clock of the ASIC. The chip for conditioning the optical signal synchronizes all input signals.

Clock 48 MHz: The timing circuit is to be terminated at the chip, in order to avoid overswings and underswings. The dimensioning in the application circuit can serve as a guide. The quality of the scan requires a pulse duty factor that is as close as possible to 50:50. The pulse symmetry of the oscillator should not be impaired because of the termination.

busya, busyb: By means of a retriggerable monoflop circuit, an LED can be connected optionally to these ports that displays the signal flow (only relevant for FOCSI 1).

Commissioning Tips:

- Isolate the chip for conditioning the optical signal from the fiber-optic network, to exclude outside influences.
- Stimulate the chip for conditioning the optical signal alternately at all three ports at the input.
- Rectangular signal 1 MHz to 6 MHz is suitable (preferably 3 / 1.5 / 0.75 MHz).
- At the respective "opposing" outputs, there must be a reaction to this signal.
- If this does not happen, the chip for conditioning the optical signal could be locked into a fixed data direction through RTSTT or interference on another input.
- Internal masking of a fiber-optic port is recognizable from the idle level of the associated Busy_Signal.
- RXPA >> busya, RXPB >> busyb.

Frequent error sources during the test phase were:

- Wrong or interchanged (RX/TX) fiber-optic components
- System blockage because of self-interference of a receiver
- Floating RTSTT (as a rule through line interruption)

11. Technical Specifications

Transmission current LED	60 mA / each LED
Permitted FO_length POF	50 m
Permitted FO_length HCS	300 m
Optical power reserve	3 dB (for maximum lengths/expanded temperature range)
Expanded temperature range, QFBR	HP components are specified correspondingly
Moisture condensation HP_FO	No electrical destruction; same-design 5MBit types are qualified. Damping in the case of condensation was measured. It is not a detriment.
Current consumption M4a64/32	App. 50 mA
Cascading depth	32 stations starting with the master (included) (2 * 32, if master is positioned topologically in the center)
Current supply	+ 3.0 V to + 3.6 V
Operating temperature	- 40 ^{o}C to + 85 ^{o}C
Ambient temperature	- 40 ^{o}C to + 85 ^{o}C

3.3-V Type:
44-pin TQFP case

Information regarding 3/5-V mixed design:
3.3-V chip has TTL_input thresholds and 3-V output swing.
All I/O on the 3-V type tolerate 5-V input levels.

All I/O have integrated pull-up resistors.

12. Time Response for Cascading

Functional Background:

- Each chip for conditioning the optical signal has a bit buffer (FIFO) to buffer quartz tolerances by means of a message frame.
- The FIFO size used is selected so that +/- 100 ppm frequency differences can be intercepted by means of a message frame of maximum length.
- First, the FIFO is filled up to 50% prior to further transmission. This provides for a reserve against underflow.
- Depending on the quartz ratio of source and sink, there is a tendency toward overflow or underflow.
- Regarding a two-way route over the segment, overflow and underflow of two partners are corrected into an average.
- Because of the retimer procedure, the digital delay caused by the chip for conditioning the optical signal does not depend on the baud rate.

Component	Delay	Explanation
Light runtime in the fiber-optic cable	5 ns/m	Is not subject to fluctuations
Analog delay through the fiber-optic components RX + TX	130ns .. 150ns	Time depends on the level. Temperature behavior not clarified.
Minimum digital delay	3.5 x 83.3ns	Pulse of the chip for conditioning the optical signal is faster than the source.
Maximum digital delay	8.5 x 83.3ns	Pulse of the chip for conditioning the optical signal is slower than the source.
Median digital delay	6.0 x 83.3ns	This value is applied to the response time on the line, request <>response. In the case of a two-way route by way of the same segment, the median value is **always** the result.

13. Cascading Depth and Standard DP Profile

In contrast to a copper segment where the stations only "tap" the signal, in the fiber-optic segment each station is a repeater. This results in increased demands on the time response of the segment.
In the case of the Std_DP profile in the configuration tool, the time reserved for the propagation delay in the system is the difference of the slot time minus tsdr_max.
The table below provides a guide regarding the cascading depth of the chip for conditioning the optical signal if there is one 50-m fiber-optic segment each between two stations and the standard DP profile timing must be adhered to in the worst case.

Baud Rate	Cascading
12 Mbaud	9 / 32 (*)
6 Mbaud	Baud rate blocked
3 Mbaud	Baud rate blocked
1.5 Mbaud	32
Rest	32

(*) 32 stations if the DP profile is adapted to the propagation delay.

As maximum cascading depth including the master, 32 is specified.

If the runtime calculation results in a cascading depth larger than 32, the valid maximum therefore is 32.

Note:
If the (mono) master of a fiber-optic system is topologically in the center, the maximum cascading depth is permitted for each fiber-optic subsegment that is connected to the master.

14. Pin Assignment for the Chip for Conditioning the Optical Signal

Name	Pin No.	Type	Attribute	Function : Signal Pin
clk48	5	in	clock, pull-up	Main clock. The clock symmetry is very important to the function of the circuit. +/-5% dissymmetry should be the objective.
res_n	31	29	In, pull-up	Power_On_Reset. Caution! Don't connect this pin with the software reset port of the ASPC2 / SPCx / DPC31 ASIC. The FOSCI (fiber-optic cable coupler) is disabled under reset. A SW driver that resets "its" ASIC because of a crash must not interrupt the line.
rxpa	42	in	pull-up	Receive Data Port A
rxpb	24	in	pull-up	Receive Data Port B
rxtt	22	in	pull-up	Receive Data Port TTL. CAUTION! Risk of confusion: Port **rx**tt is wired to the signal **tx**d of the ASIC.
rtstt	2	in	pull-up	RTS, send request by the DP ASIC. If not used, low-resistance pulldown resistor required (1 K).
reti	34	in	pull-down	
txpa	15	out	active	Transmit data to Port A
txpb	19	out	active	Transmit data to Port B
txtt	13	out	active	Transmit data to Port TTL. CAUTION! Risk of confusion: Port **tx**tt is wired to the signal **rx**d of the ASIC.
busya	25	out	active	Trigger signal for a Startup_LED Channel A; refer to standard application. (only relevant for FOCSI 1)
busyb	35	out	active	Same as busya
VCC	16,38			Positive supply voltage 5 V
GND	6,17, 28,39			"Ground" supply of chip
Not used I/O	Remainder	in	pull-up	**The connections remain open on the module.**