S7-400H Instruction List

CPU 412-3H, 414-4H, 417-4H

Edition 09/2007

A5E01359153-01

Siemens AG
Bereich Automation and Drives
Geschaeftsgebiet Industrial Automation Systems
Postfach 4848, D- 90327 Nuernberg

Disclaimer of Liability

We have checked the contents of this manual for agreement with the hardware and software described. Since deviations cannot be precluded entirely, we cannot guarantee full agreement. However, the data in this manual are reviewed regularly and any necessary corrections included in subsequent editions. Suggestions for improvement are welcomed.

Siemens Aktiengesellschaft

A5E01359153-01

Contents

Applicability

This list of instructions applies to the CPUs listed below.

Name	Order number
CPU 412-3H	6ES7412-3HJ14-0AB0
CPU 414-4H	6ES7414-4HM14-0AB0
CPU 417-4H	6ES7417-4HT14-0AB0

Address Identifier and Parameter Ranges

Addr. ID	Parameter Range			Description
	CPU 412-3H	CPU 414-4H	CPU 417-4H	
Q1[1)]	0.0 to 255.7	0.0 to 255.7	0.0 to 1023.7	Output (in PIQ)
QB1[1)]	0 to 255	0 to 255	0 to 1023	Output byte (in PIQ)
QW1[1)]	0 to 254	0 to 254	0 to 1022	Output word (in PIQ)
QD1[1)]	0 to 252	0 to 252	0 to 1020	Output double word (in PIQ)
DBX	0.0 to 65533.7	0.0 to 65533.7	0.0 to 65533.7	Data bit in data block
DB	1 to 4095	1 to 4095	1 to 8191	Data block
DBB	0 to 65533	0 to 65533	0 to 65533	Data byte in DB
DBW	0 to 65532	0 to 65532	0 to 65532	Data word in DB
DBD	0 to 65530	0 to 65530	0 to 65530	Data double word in DB
DIX	0.0 to 65533.7	0.0 to 65533.7	0.0 to 65533.7	Data bit in instance DB
DI	1 to 4095	1 to 4095	1 to 8191	Instance data block
DIB	0 to 65533	0 to 65533	0 to 65533	Data byte in instance DB
DIW	0 to 65532	0 to 65532	0 to 65532	Data word in instance DB
DID	0 to 65530	0 to 65530	0 to 65530	Data double word instance DB

1) Default setting can be changed, see Technical Specifications

Address Identifier and Parameter Ranges, continued

Addr. ID	Parameter Range CPU 412-3H	CPU 414-4H	CPU 417-4H	Description
I[2)]	0.0 to 255.7	0.0 to 255.7	0.0 to 1023.7	Input bit (in PII)
IB[2)]	0 to 255	0 to 255	0 to 1023	Input byte (in PII)
IW[2)]	0 to 254	0 to 254	0 to 1022	Input word (in PII)
ID[2)]	0 to 252	0 to 252	0 to 1020	Input double word (in PII)
L[2)]	0.0 to 8191.7	0.0 to 8191.7	0.0 to 32767.7	Local data
LB[2)]	0 to 8191	0 to 8191	0 to 32767	Local data byte
LW[2)]	0 to 8191	0 to 8190	0 to 32766	Local data word
LD[2)]	0 to 8191	0 to 8188	0 to 32764	Local data double word
M	0.0 to 8191.7	0.0 to 8191.7	0.0 to 16383.7	Bit memory
MB	0 to 8191	0 to 8191	0 to 16383	memory byte
MW	0 to 8190	0 to 8190	0 to 16382	memory word
MD	0 to 8188	0 to 8188	0 to 16380	memory double word

2) Default setting can be changed, see Technical Specifications

Address Identifier and Parameter Ranges, continued

Addr. ID	Parameter Range CPU 412-3H	CPU 414-4H	CPU 417-4H	Description
PQB	0 to 8191	0 to 8191	0 to 16383	Peripheral output byte (direct I/O access)
PQW	0 to 8190	0 to 8190	0 to 16382	Peripheral output word (direct I/O access)
PQD	0 to 8188	0 to 8188	0 to 16380	Peripheral output double word (direct I/O access)
PIB	0 to 8191	0 to 8191	0 to 16383	Peripheral input byte (direct I/O access)
PIW	0 to 8190	0 to 8190	0 to 16382	Peripheral input word (direct I/O access)
PID	0 to 8188	0 to 8188	0 to 16380	Peripheral output double word (direct I/O access)
T	0 to 2047	0 to 2047	0 to 2047	Timer
C	0 to 2047	0 to 2047	0 to 2047	Counter

Constants and Ranges

Constant	Range	Description
B(b1,b2) B(b1,b2,b3,b4)	–	Constant, 2 or 4 bytes
D# Date	–	IEC date constant
L# Integer	–	32-bit integer constant
P# Bit pointer	–	Pointer constant
S5T# Time value	–	S7 time constant [1]
T# TIme value	—	Time constant
TOD# Time value	–	IEC time constant
C# Count value	–	Counter constant (BCD code)
2#n	–	Binary constant
B#16# W#16# DW#16#	–	Hexadecimal constant

1) For loading of S7 timers.

Abbreviations and Mnemonics

The following abbreviations and mnemonics are used in the Instruction List:

Abbrev.	Description	Example
k8	8-bit constant 0 to 255	32
k16	16-bit constant 256 to 32 767	28 131
k32	32-bit constant 32 768 to 999 999 999	127 624
i8	8-bit integer -128 to +127	-113
i16	16-bit integer -32768 to +32767	+6523
i32	32-bit integer -2 147 483 648 to +2 147 483 647	-2 222 222
m	Pointer constant	P#240.3
n	Binary constant	1001 1100
p	Hexadecimal constant	EA12
Label	Symbolic jump address (max. 4 characters)	DESTINATION
a	Byte address	

Abbreviations and Mnemonics, continued

Abbrev.	Description	Example
b	Bit address	
c	Address area	I, Q, M, L, DBX, DIX
d	Address in: MD, DBD, DID or LD	
e	Number in: MW, DBW, DIW or LW	
f	Timer/counter No.	
g	Address area	IB, QB, PIB, PQB, MB, LB, DBB, DIB
h	Address area	IW, QW, PIW, PQW, MW, LW, DBW, DIW
i	Address area	ID, QD, PID, PQD, MD, LD, DBD, DID
q	Block No.	

Registers

ACCU1 to ACCU4 (32 Bits)

The accumulators are registers for processing bytes, words or double words. The address identifiers are loaded into the accumulators, where they are logically gated. The result of the logic operation (RLO) is in ACCU1 and can be transferred from there to a memory cell.

The accumulators are 32 bits long.

Accumulator designations :

ACCU	Bits
ACCUx (x = 1 to 4)	Bit 0 to 31
ACCUx-L	Bit 0 to 15
ACCUx-H	Bit 16 to 31
ACCUx-LL	Bit 0 to 7
ACCUx-LH	Bit 8 to 15
ACCUx-HL	Bit 16 to 23
ACCUx-HH	Bit 24 to 31

Address Registers AR1 and AR2 (32 Bits)

The address registers contain the area-internal or area-crossing pointers for instructions using indirect addressing. The address registers are 32 bits long.

The area-internal and/or area-crossing pointers have the following syntax:

- Area-internal pointer `00000000 00000bbb bbbbbbbb bbbbbxxx`
- Area-crossing pointer **`yyyyyyyy`** `00000bbb bbbbbbbb bbbbbxxx`

Legend:

`b`	Byte address
`x`	Bit number
`y`	Area identifier (see “Examples of Addressing”)

Status Word (16 Bits)

The status word bits are evaluated or set by the instructions.

The status word is 16 bits long.

Bit	Assignment	Description
0	/FC	First check bit
1	RLO	Result of logic operation
2	STA	Status
3	OR	Or (AND before OR)
4	OS	Stored overflow
5	OV	Overflow
6	CC 0	Condition code 0
7	CC 1	Condition code 1
8	BR	Binary result
9 to 15	Unassigned	–

Examples of Addressing

Addressing Examples	Description
Immediate Addressing	
L +27	Load 16-bit integer constant “27” into ACCU1
L L#-1	Load 32-bit integer constant “-1” into ACCU1
L 2#1010101010101010	Load binary constant into ACCU1
L DW#16#A0F0BCFD	Load hexadecimal constant into ACCU1
L ’ENDE’	Load ASCII character into ACCU1
L T#500 ms	Load time value into ACCU1
L C#100	Load count value into ACCU1
L B#(100,12)	Load 2-byte constant
L B#(100,12,50,8)	Load 4-byte constant
L P#10.0	Load area-internal pointer into ACCU1
L P#E20.6	Load area-crossing pointer into ACCU1
L -2.5	Load real number into ACCU1
L D# 1995-01-20	Load date
L TOD 13:20:33.125	Load time of day

Addressing Examples	Description
Direct Addressing	
A I 0.0	ANDing of input bit 0.0
L IB 1	Load input byte 1 into ACCU1
L IW 0	Load input word 0 into ACCU1
L ID 0	Load input double word 0 into ACCU1
Indirect Addressing of Timers/Counters	
SP T [LW 8]	Start timer; the timer number is in local data word 8
CU C [LW 10]	Count upwards; the counter number is in local data word 10
Area-Internal Memory-Indirect Addressing	
A I [LD 12] Example: L P#22.2 T LD 12 A I [LD 12]	AND operation: The address of the input is in local data double word 12 as pointer
A I [DBD 1]	AND operation: The address of the input is in data double word 1 of the open DB as pointer
A I [DID 12]	AND operation: The address of the output is in data double word 12 of the open instance DB as pointer
A I [MD 12]	AND operation: The address of the output is in memory double word 12 as pointer

Examples of Addressing, continued

Addressing Examples
Area-Internal Register-Indirect Addressing
A I [AR1,P#12.2]
Area-Crossing Register-Indirect Addressing

For area-crossing register-indirect addressing, the address must also contain an area identifier. The address is in the address register. The area identifiers are as follows:

Area identifier	Coding (binary)	hex.	Area
P	1000 0**000**	80	I/O area
I	1000 0**001**	81	Input area
Q	1000 0**010**	82	Output area
M	1000 0**011**	83	Bit memory area
DB	1000 0**100**	84	Data area
DI	1000 0**101**	85	Instance data area
L	1000 0**110**	86	Local data area
VL	1000 0**111**	87	Predecessor local data area (access to local data of invoking block)

L B [AR1,P#8.0]	Load byte into ACCU1: The address is calculated from the “pointer value in AR 1 + P#8.0”
A [AR1,P#32.3]	AND operation: The address of the operand is calculated from the “pointer value in AR 1 + P#32.3”
Addressing Via Parameters	
A Parameter	Addressing via parameters

Examples of how to calculate the pointer

- **Example for sum of bit addresses ≦7:**

  LAR1 P#8.2
  A I [AR1,P#10.2]

Result: Input 18.4 is addressed (by adding the byte and bit addresses)

- **Example for sum of bit addresses >7:**

  L P#10.5
  LAR1
  A I [AR1,P#10.7]

Result: Input 21.4 is addressed (by adding the byte and bit addresses with carry over)

Execution Times with Indirect Addressing

When using indirect addresses statement consists of two parts:

Part 1: Load the address of the instruction

Part 2: Execute the instruction

In other words, when working with indirect addresses, you must calculate the execution time of an instruction from these two parts.

Calculating the Execution Time

The total execution time is calculated as follows:

	Time required for loading the address
+	execution time of the instruction
=	Total execution time of the instruction

The execution times listed in the chapter entitled “List of Instructions” apply to the execution times of the second part of an instruction, i.e. for the actual execution of an instruction.

You must then add the time required for loading the address of the instruction to this execution time (see following Table).

The execution time for loading the address of the instruction from the various areas is shown in the following table.

Address is in ...	Execution Time in ns		
	CPU 412-3H	**CPU 414-4H**	**CPU 417-4H**
Bit memory area M Word Double word	 150 150	 90 90	 36 36
Data block DB/DX Word Double word	 175 175	 105 105	 42 42
Local data area L Word Double word	 150 150	 90 90	 36 36
AR1/AR2 (area-internal)	0.0 [1]	0.0 [1]	0.0 [1]
AR1/AR2 (area-crossing)	0.0 [1]	0.0 [1]	0.0 [1]
Parameter (word) ... for: • Timers • Counters • Block calls	 175 175 175	 105 105 105	 42 42 42
Parameter (double word) ... for Bits, bytes, words and double words	175	105	42

[1] Address registers AR1/AR2 do not need to be loaded in separate cycles for addressing.

The pages that follow contain examples for calculating the instruction run time for the various indirectly addressed instructions.

Examples of Calculations

You will find a few examples here for calculating the execution times for the various methods of indirect addressing.

Calculating the Execution Times for Area-Internal Memory-Indirect Addressing

Example: A I [DBD 12] with CPU 414

Step 1: Load the contents of DBD 12 (time required is listed in the table on page 20)

Address is in ...	Execution Time in ns
Bit memory area M Word Double word	 90 90
Data block DB/DX Word Double word	 105 105

Step 2: AND the input addressed in this way (you will find the execution time in the tables in the chapter entitled “List of Instructions” on page 25)

Typical Execution Time in ns	
Direct Addressing	**Indirect Addressing**
45 :	Time for A I **45+** **:**

Total execution time:

105 ns
\+ 45 ns
150 ns

Execution Time for Area-Crossing Register-Indirect Addressing

Example: A [AR1, P#23.1] ... with I 1.0 in AR1 with CPU 416

Step 1: Load the contents of AR1, and increment them by the offset 23.1 (the time required is in the table on page 20)

Address is in ...	Execution Time in ns
:	:
AR1/AR2 (area-crossing)	0.00
:	:

Step 2: AND link of the input addressed this way (see page 25 for the execution time)

Typical Execution Time in ns	
Direct Addressing	**Indirect Addressing**
30 :	Time for A I **30+** **:**

Total execution time:

0.0 ns
+ 30 ns
30 ns

List of Instructions

This chapter contains the complete list of instructions for the S7-400 CPUs. The descriptions have been kept as concise as possible. You will find a detailed functional description in the various STEP 7 reference manuals.
Please note that, in the case of indirect addressing (examples see page 16), you must add the time required for loading the address of the particular instruction to the execution times listed (see page 19).

Bit Logic Instructions

All logic instructions generate a result (new RLO). The first instruction in a logic string generates the new RLO from the signal state scanned. The subsequent logic instructions generate the new RLO from the signal state scanned and the old RLO. The logic string ends with an instruction which limits the RLO (e.g. a memory instruction); that is, the /FC bit is set to zero.

Instr.	Address ID	Description	Length in Words	Execution Time in ns		
				CPU 412-3H	CPU 414-4H	CPU 417-4H
U/UN						
	I/Q a.b	Input/output	1[1]/2	75	45	18
	M a.b	Bit memory	1[2]/2	75	45	18
	L a.b	Local data bit	2	75	45	18
	DBX a.b	Data bit	2	100	60	24
	DIX a.b	Instance data bit	2	100	60	24
	c [d]	Memory-indirect, area-internal[3]	2	75+/100+	45+/60+	18+/24+
	c [AR1,m]	Register-ind., area-internal (AR1)[3]	2	75+/100+	45+/60+	18+/24+
	c [AR2,m]	Register-ind., area-internal (AR2)[3]	2	75+/100+	45+/60+	18+/24+
	[AR1,m]	Area-crossing (AR1)[3]	2	75+/100+	45+/60+	18+/24+
	[AR2,m]	Area-crossing (AR2)[3]	2	75+/100+	45+/60+	18+/24+
	Parameter	Via parameter [3]	2	75+/100+	45+/60+	18+/24+

Statusword for: **U/UN**	BIE	A1	A0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	–	–	–	–	–	Yes	–	Yes	Yes
Instruction affects:	–	–	–	–	–	Yes	Yes	Yes	1

\+ Plus time required for loading the address of the instruction (see page 20)

1) With direct instruction addressing;Address area 0 to 127

2) With direct instruction addressing;Address area 0 to 255

3) I,Q,M,L / DB, DI

Bit Logic Instructions, continued

Instr.	Address ID	Description	Length in Words	Execution Time in ns		
				CPU 412-3H	CPU 414-4H	CPU 417-4H
O/ON		OR/OR-NOT				
	I/Q a.b	Input/output	1[1)]/2	75	45	18
	M a.b	Bit memory	1[2)]/2	75	45	18
	L a.b	Local da	2	75	45	18
	DBX a.b	Data bit	2	100	60	24
	DIX a.b	Instance data bit	2	100	60	24
	c [d]	Memory-indirect, area-internal [3)]	2	75+/100+	45+/60+	18+/24+
	c [AR1,m]	Register-ind., area-internal (AR1) [3)]	2	75+/100+	45+/60+	18+/24+
	c [AR2,m]	Register-ind., area-internal (AR2) [3)]	2	75+/100+	45+/60+	18+/24+
	[AR1,m]	Area-crossing (AR1) [3)]	2	75+/100+	45+/60+	18+/24+
	[AR2,m]	Area-crossing (AR2) [3)]	2	75+/100+	45+/60+	18+/24+
	Parameter	Via parameter [3)]	2	75+/100+	45+/60+	18+/24+

Statusword for: **O, ON**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	Yes	Yes
Instruction affects:	–	–	–	–	–	0	Yes	Yes	1

\+ Plus time required for loading the address of the instruction (see page 20)

1) With direct instruction addressing; Address area 0 to 127

2) With direct instruction addressing; Address area 0 to 255

3) I,Q,M,L / DB, DI

Bit Logic Instructions, continued

Instr.	Address-ID	Description	Length in Words	Execution Time in ns		
				CPU 412-3H	CPU 414-4H	CPU 417-4H
X/XN		EXKLUSIV-OR/ EXKLUSIV-OR-NOT				
	E/A a.b	Input/output	2	75	45	18
	M a.b	Bit memory	2	75	45	18
	L a.b	Local data bit	2	75	45	18
	DBX a.b	Data bit	2	100	60	24
	DIX a.b	Instance data bit	2	100	60	24
	c [d]	Memory-indirect, area-internal. 1)	2	75+/100+	45+/60+	18+/24+
	c [AR1,m]	Register-ind., area-internal (AR1) 1)	2	75+/100+	45+/60+	18+/24+
	c [AR2,m]	Register-ind., area-internal (AR2) 1)	2	75+/100+	45+/60+	18+/24+
	[AR1,m]	Area-crossing (AR1) 1)	2	75+/100+	45+/60+	18+/24+
	[AR2,m]	Area-crossing (AR2) 1)	2	75+/100+	45+/60+	18+/24+
	Parameter	Via parameter 1)	2	75+/100+	45+/60+	18+/24+

Status word for: **X, XN**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	Yes	Yes
Instruction affects:	–	–	–	–	–	0	Yes	Yes	1

+Plus time required for loading the address of the instruction (see page 20)

1) I,Q,M,L / DB, DI

Bit Logic Instructions with Parenthetical Expressions

Saving the RLO and OR bits and the relevant function identifier (A, AN, ...) to the nesting stack. Seven nesting levels are possible per block. After the right parenthesis, the logic operation indicated by the function identifier is performed on the saved RLO and the current RLO; the current OR is overwritten with the saved OR.

In-struc-tion	Address ID	Description	Length in Words	Execution Time in ns		
				CPU 412-3H	CPU 414-4H	CPU 417-4H
U(		AND left parenthesis	1	75	45	18
UN(		AND NOT left parenthesis	1	75	45	18
O(		OR left parenthesis	1	75	45	18
ON(		OR NOT left parenthesis	1	75	45	18
X(		Exclusive OR left parenthesis	1	75	45	18
XN(		EXKLUSIV-ODER-NICHT-Klam-parenthesis	1	75	45	18

Statusword for: **U(, UN(, O(, ON(, X(, XN(**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	Yes	–	Yes	Yes
Instruction affects:	–	–	–	–	–	0	1	–	0

Bit Logic Instructions with Parenthetical Expressions, continued

In-struc-tion	Address ID	Description	Length in Words	Execution Time in ns		
				CPU 412-3H	CPU 414-4H	CPU 417-4H
)		Right parenthesis, removing an entry from the nesting stack.	1	75	45	18

Statusword for: **)**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	Yes	–
Instruction affects:	–	–	–	–	–	Yes	1	Yes	1

ORing of AND Instructions

The ORing of AND instructions is implemented according to the rule: AND before OR.

Instruction	Address ID	Description	Length in Words	Execution Time in ns		
				CPU 412-3H	CPU 414-4H	CPU 417-4H
O		ORing of AND operations according to the rule: AND before OR	1	75	45	18

Status word for: **O**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	Yes	Yes
Instruction affects:	–	–	–	–	–	Yes	1	–	Yes

Logic Instructions with Timers and Counters

Examining the status of the addressed timer/counter and gating the result with the RLO according to the appropriate logic function.

Instruction	Address ID	Description	Length in Words	Execution Time in ns		
				CPU 412-3H	CPU 414-4H	CPU 417-4H
A/AN		AND/AND NOT				
	T f	Timer	1[1)]/2	75	45	18
	T [e]	Timer, memory-indirect addressing	2	75+	45+	18+
	C f	Counter	1[1)]/2	75	45	18
	C [e]	Counter, memory-indirect addressing	2	75+	45+	18+
	Timerpara. Counter para.	Timer/counter (addressing via parameter)	2	75+ 75+	45+ 45+	18+ 18+

Status word for: **A, AN**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	Yes	–	Yes	Yes
Instruction affects:	–	–	–	–	–	Yes	Yes	Yes	1

\+ Plus time required for loading the address of the instruction (see page 20)

1) With direct instruction addressing ;Address area 0 to 255

Logic Instructions with Timers and Counters, continued

Instruction	Address ID	Description	Length in Words	Execution Time in ns		
				CPU 412-3H	CPU 414-4H	CPU 417-4H
O/ON						
	T f	Timer	1[1)]/2	75	45	18
	T [e]	Timer, memory-indirect addr.	2	75+	45+	18+
	C f	Counter	1[1)]/2	75	45	18
	C [e]	Counter, memory-indirect addressing	2	75+	45+	18+
	Timerpara. Counterpara.	Timer/counter (addressing via parameter)	2	75+ 75+	45+ 45+	18+ 18+
X/XN		EXCLUSIVE OR/EXCLUSIVE OR NOT				
	T f	Timer	2	75	45	18
	T [e]	Timer, memory-indirect addr.	2	75+	45+	18+
	C f	Counter	2	75	45	18
	C [e]	Counter, mem.-indirect addr.	2	75+	45+	18+
	Timerpara. Counterpara.	EXCLUSIVE OR timer/counter (addressing via parameter)	2	75+ 75+	45+ 45+	18+ 18+

Status word for: **O, ON, X, XN**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	Yes	Yes
Instruction affects:	–	–	–	–	–	0	Yes	Yes	1

\+ Plus time required for loading the address of the instruction (see page 20)

1) With direct instruction addressing; address area 0 to 255

Word Logic Instructions with the Contents of Accumulator 1

Gating the contents of ACCU1 and/or ACCU1-L with a word or double word according to the appropriate function. The word or double word is either specified in the instruction as an address or is in ACCU2. The result is in ACCU1 and/or ACCU1-L.

In-struc-tion	Address ID	Description	Length in Words	Execution Time in ns		
				CPU 412-3H	CPU 414-4H	CPU 417-4H
AW		AND ACCU2-L	1	75	45	18
AW	W#16#p	AND 16-bit constant	2	75	45	18
OW		OR ACCU2-L	1	75	45	18
OW	W#16#p	OR 16-bit constant	2	75	45	18
XOW		EXCLUSIVE OR ACCU2-L	1	75	45	18
XOW	W#16#p	EXKLUSIV-ODER EXCLUSIVE OR 16-bit constant	2	75	45	18

Status word for: **UW, OW, XOW**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	ja	0	0	–	–	–	–	–

Word Logic Instructions with the Contents of Accumulator 1, continued

Instruction	Address ID	Description	Length in Words	Execution Time in ns		
				CPU 412-3H	CPU 414-4H	CPU 417-4H
AD		AND ACCU2	1	75	45	18
AD	DW#16#p	AND 32-bit constant	3	113	68	27
OD		OR ACCU2	1	75	45	18
OD	DW#16#p	OR 32-bit constant	3	113	68	27
XOD		EXCLUSIVE OR ACCU2	1	75	45	18
XOD	DW#16#p	EXCLUSIVE OR 32-bit constant	3	113	68	27

Status word for: **UD, OD, XOD**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	Yes	0	0	–	–	–	–	–

Evaluating Conditions Using AND, OR and EXCLUSIVE OR

All logic instructions generate a result (new RLO). The first instruction in a logic string generates the new RLO from the signal state scanned. The subsequent logic instructions generate the new RL from the signal state scanned and the old RLO. The logic string ends with an instruction which limits the RLO (e.g. a memory instruction); that is, the $\overline{FC}$ bit is set to zero.

Instruction	Address ID	Description	Length in Words	Execution Time in ns		
				CPU 412-3H	CPU 414-4H	CPU 417-4H
A/AN O/ON X/XN	==0	AND/AND NOT OR/OR-NOT EXCLUSIVE OR/ EXCLUSIVE-OR-NOT Result=0 (A1=0 and A0=0)	1	75	45	18
	>0	Result>0 (CC1=1 and CC0=0)	1	75	45	18
	<0	Result<0 (CC1=0 and CC0=1)	1	75	45	18
	<>0	Result≠0 ((CC1=0 and CC0=1) or (CC1=1 and CC0=0))	1	75	45	18

Status word for: **A/AN/O/ON/X/XN**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	Yes	Yes	–	–	Yes	–	Yes	Yes
Instruction affects:	–	–	–	–	–	Yes	Yes	Yes	1

Evaluating Conditions Using AND, OR and EXCLUSIVE OR, continued

Instruction	Address ID	Description	Length in Words	Execution Time in ns		
				CPU 412-3H	CPU 414-4H	CPU 417-4H
A/AN O/ON X/XN	>=0	Result>=0 ((CC1=1 and CC0=0) or (CC1=0 and CC0=0))	1	75	45	18
	<=0	Result<=0 ((CC1=0 and CC0=1) or (CC1=0 and CC0=0))	1	75	45	18

Status word for: **A/AN/O/ON/X/XN**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	Yes	Yes	–	–	Yes	–	Yes	Yes
Instruction affects:	–	–	–	–	–	Yes	Yes	Yes	1

Evaluating Conditions Using AND, OR and EXCLUSIVE OR, continued

Instruction	Address ID	Description	Length in Words	Execution Time in ns		
				CPU 412-3H	CPU 414-4H	CPU 417-4H
A/AN O/ON X/XN	UO	AND/AND-NOT OR/OR-NOT EXCLUSIVE-OR/ EXCLUSIVE-OR-NOT Unordered math instruction (CC1=1 and CC0=1)	1	75	45	18
	OS	AND OS=1	1	75	45	18
	BR	AND BR=1	1	75	45	18
	OV	AND OV=1	1	75	45	18

Status word for: **A/AN/O/ON/X/XN**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	Yes	Yes	Yes	Yes	Yes	Yes	–	Yes	Yes
Instruction affects:	–	–	–	–	–	Yes	Yes	Yes	1

Edge-Triggered Instructions

The current RLO is compared with the status of the instruction or “edge bit memory”. FP detects a change from “0” to “1”; FN detects a change from “1” to “0”.

Instruction	Address ID	Description	Length in Words	Execution Time in ns		
				CPU 412-3H	CPU 414-4H	CPU 417-4H
FP/FN	I/Q a.b M a.b L a.b1) DBX a.b DIX a.b c [d] c [AR1,m] 2) c [AR2,m] 2) [AR1,m] 2) [AR2,m] 2) Parameter 2)	The positive/negative edge is indicated by RLO = 1. The bit addressed in the instruction is the auxiliary edge bit memory.	2 2 2 2 2 2 2 2 2 2 2	75 75 75 200 200 75+/200+ 75+/200+ 75+/200+ 75+/200+ 75+/200+ 75+/200+	45 45 45 120 120 45+/120+ 45+/120+ 45+/120+ 45+/120+ 45+/120+ 45+/120+	18 18 18 48 48 18+/48+ 18+/48+ 18+/48+ 18+/48+ 18+/48+ 18+/48+

Status word for: **FP, FN**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	Yes	–
Instruction affects:	–	–	–	–	–	0	Yes	Yes	1

\+ Plus time required for loading the address of the instruction (see page 20)
1) Unnecessary if the bit being monitored is in the process image (local data of a block are only valid while the block is running).
2) I, Q, M, L /DB, DI

Setting/Resetting Bit Addresses

Assigning the value “1” or “0” to the addressed instruction when RLO = 1. The instructions can be dependent on the MCR (see page 97).

ration Instruc-tion	Address ID	Description	Length in Words	Execution Time in ns		
				CPU 412-3H	CPU 414-4H	CPU 417-4H
S		Set addressed bit to “1”				
R		Set addressed bit to “0”				
	I/Q a.b	Input/output	1[1)]/2	75	45	18
	M a.b	Bit memory	1[2)]/2	75	45	18
	L a.b	Local data bit	2	75	45	18
	DBX a.b	Data bit	2	200	120	48
	DIX a.b	Instance data bit	2	200	120	48
	c [d]	Memory-indirect, area-internal [3)]	2	75+/200+	45+/120+	18+/48+
	c [AR1,m]	Register-indirect, area-internal (AR1) [3)]	2	75+/200+	45+/120+	18+/48+
	c [AR2,m]	Register-indirect, area-internal (AR2) [3)]	2	75+/200+	45+/120+	18+/48+
	[AR1,m]	Area-crossing (AR1) [3)]	2	75+/200+	45+/120+	18+/48+
	[AR2,m]	Area-crossing (AR2) [3)]	2	75+/200+	45+/120+	18+/48+
	Parameter	Via parameter	2	75+/200+	45+/120+	18+/48+

Status word for: **S, R**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	Yes	–
Instruction affects:	–	–	–	–	–	0	Yes	–	0

\+ Plus time required for loading the address of the instruction (see page 20)
1) With direct instruction addressing; Address area 0 to 127
2) With direct instruction addressing; Address area 0 to 255
3) I, Q, M, L / DB, DI

Setting/Resetting Bit Addresses, continued

The RLO is written to the address of the instruction. The instructions can be dependent on the MCR (see page 97).

Instru Ction	Address ID	Description	Length in Words	Execution Time in ns		
				CPU 412-3H	CPU 414-4H	CPU 417-4H
=		Assign RLO				
	I/Q a.b	To input/output	1[1)]/2	75	45	18
	M a.b	To bit memory	1[2)]/2	75	45	18
	L a.b	To local data bit	2	75	45	18
	DBX a.b	To data bit	2	200	120	48
	DIX a.b	To instance data bit	2	200	120	48
	c [d]	Memory-indirect, area-internal [3)]	2	75+/200+	45+/120+	18+/48+
	c [AR1,m]	Register-indirect, area-internal (AR1) [3)]	2	75+/200+	45+/120+	18+/48+
	c [AR2,m]	Register-indirect, area-internal (AR2) [3)]	2	75+/200+	45+/120+	18+/48+
	[AR1,m]	Area-crossing (AR1) [3)]	2	75+/200+	45+/120+	18+/48+
	[AR2,m]	Area-crossing (AR2) [3)]	2	75+/200+	45+/120+	18+/48+
	Parameter	Via parameter [3)]	2	75+/200+	45+/120+	18+/48+

Status word for: =	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	Yes	–
Instruction affects:	–	–	–	–	–	0	Yes	–	0

\+ Plus time required for loading the address of the instruction (see page 20)
1) With direct instruction addressing; Address area 0 to 127
2) With direct instruction addressing; Address area 0 to 255
3) . I, Q, M, L / DB, DI

Instructions Directly Affecting the RLO

The following instructions have a direct effect on the RLO.

Instruction	Address ID	Description	Length in Words	Execution Time in ns		
				CPU 412-3H	CPU 414-4H	CPU 417-4H
CLR		Set RLO to “0”	1	75	45	18

Status word for: **CLR**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	–	–	–	–	0	0	0	0

SET		Set RLO to “1”	1	75	45	18

Status word for: **SET**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	–	–	–	–	0	1	1	0

NOT		Negate RLO	1	75	45	18

Status word for: **NOT**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	Yes	–	Yes	–
Instruction affects:	–	–	–	–	–	–	1	Yes	–

SAVE		Save RLO to the BR bit	1	75	45	18

Status word for: **SAVE**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	Yes	–
Instruction affects:	Yes	–	–	–	–	–	–	–	–

Timer Instructions

Starting or resetting a timer. The time value must be in ACCU1-L. The instructions are triggered by an edge transition in the RLO; that is, when the status of the RLO has changed between two calls.

In-struc-tion	Address ID	Description	Length in Words	Execution Time in ns		
				CPU 412-3H	CPU 414-4H	CPU 417-4H
SP	T f T [e]	Start timer as pulse on edge change from “0” to “1”	1[1)]/2	150 150+	90 90+	36 36+
	Timer para.		2	150+	90+	36+
SE	T f T [e]	Start timer as extended pulse on edge change from “0” to “1”	1[1)]/2	150 150+	90 90+	36 36+
	Timer para.		2	150+	90+	36+
SD	T f T [e]	Start timer as ON delay on edge change from “0” to “1”	1[1)]/2	150 150+	90 90+	36 36+
	Timer para.		2	150+	90+	36+

Status word for **SP, SE, SD**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	Yes	–
Instruction affects:	–	–	–	–	–	0	–	–	0

\+ Plus time required for loading the address of the instruction (see page 20)
1) With direct instruction addressing Timer No.: 0 to 255

Timer Instructions, continued

In-struc-tion	Address ID	Description	Length in Words	Execution Time in ns		
				CPU 412-3H	CPU 414-4H	CPU 417-4H
SS	T f T [e]	Start timer as retentive ON delay on edge change from “0” to “1”	1[1)]/2	150 150+	90 90+	36 36+
	Timer para.		2	150+	90+	36+
SF	T f T [e]	Start timer as OFF delay on edge change from “0” to “1”	1[1)]/2	150 150+	90 90+	36 36+
	Timer para.		2	150+	90+	36+

Status word for **SS, SF**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	Yes	–
Instruction affects:	–	–	–	–	–	0	–	–	0

Timer Instructions, continued

Instruction	Address ID	Description	Length in Words	Execution Time in ns		
				CPU 412-3H	CPU 414-4H	CPU 417-4H
FR	T f T [e]	Enable timer for restarting on edge change from “0” to “1” (reset edge bit memory for starting timer)	1[1)]/2	150 150+	90 90+	36 36+
	Timer para.		2	150+	90+	36+
R	T f T [e]	Reset timer	1[1)]/2	150 150+	90 90+	36 36+
	Timer para.		2	150+	90+	36

Status word for: **FR, R**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	Yes	–
Instruction affects:	–	–	–	–	–	0	–	–	0

\+ Plus time required for loading the address of the instruction (see page 20)
1) With direct instruction addressing Timer No.: 0 to 255

Counter Instructions

The count value must be in ACCU1-L in the form of a BCD number (0 - 999).

In-struc-tion	Address ID	Description	Length in Words	Execution Time in ns		
				CPU 412-3H	CPU 414-4H	CPU 417-4H
S	C f C [e]	Presetting of counter on edge change from “0” to “1”	1[1])/2	150 150+	90 90+	36 36+
	Counter para.		2	150+	90+	36+
R	C f C [e]	Reset counter to “0” when RLO = “1”	1[1])/2	150 150+	90 90+	36 36+
	Counter para.		2	150+	90+	36+
CU	C f C [e]	Increment counter by 1 on edge change from “0” to “1”	1[1])/2	150 150+	90 90+	36 36+
	Counter para.		2	150+	90+	36+

Status word for: **S, R, CU**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	Yes	–
Instruction affects:	–	–	–	–	–	0	–	–	0

\+ Plus time required for loading the address of the instruction (see page 20)
1) With direct instruction addressing Counter No.: 0 to 255

Counter Instructions, continued

In-struc-tion	Address ID	Description	Length in Words	Execution Time in ns		
				CPU 412-3H	CPU 414-4H	CPU 417-4H
CD	C f C [e]	Decrement counter by 1 on edge change from “0” to “1”	1[1)]/2	150 150+	90 90+	36 36+
	Counter para.		2	150+	90+	36+
FR	C f C [e]	Enable counter on edge change from “0” to “1” (reset edge bit memory for up and down counting and setting the counter)	1[1)]/2	150 150+	90 90+	36 36+
	Counter para.		2	150+	90+	36+

Status word for: **CD, FR**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	Yes	–
Instruction affects:	–	–	–	–	–	0	–	–	0

\+ Plus time required for loading the address of the instruction (see page 20)
1) With direct instruction addressing Counter No.: 0 to 255

Load Instructions

Loading address identifiers into ACCU1. The contents of ACCU1 are first saved to ACCU2. The status word is not affected.

Instruction	Address ID	Description	Length in Words	Execution Time in ns		
				CPU 412-3H	CPU 414-4H	CPU 417-4H
L		Load ...				
	IB a	Input byte	1[1])/2	75	45	18
	QB a	Output byte	1[1])/2	75	45	18
	PIB a	Peripheral input byte (solo [2])	1[1])/2	75	45	18
		Peripheral-input byte (redundant)	1[1])/2	33 µs	22 µs	12 µs
	MB a	Bit memory byte	1[3])/2	75	45	18
	LB a	Local data byte	2	75	45	18
	DBB a	Data byte	2	100	60	24
	DIB a	Instance data byte	2	100	60	24
		... into ACCU1				
	g [d]	Memory-indirect, area-internal [4]	2	75+/100+	45+/60+	18+/24+
	g [AR1,m]	Register-indirect, area-internal (AR1) [4]	2	75+/100+	45+/60+	18+/24+
	g [AR2,m]	Register-indirect, area-internal (AR2) [4]	2	75+/100+	45+/60+	18+/24+
	B[AR1,m]	Area-crossing (AR1) [4]	2	75+/100+	45+/60+	18+/24+
	B[AR2,m]	Area-crossing (AR2) [4]	2	75+/100+	45+/60+	18+/24+
	Parameter	Via parameter [4]	2	75+/100+	45+/60+	18+/24+

\+ Plus time required for loading the address of the instruction (see page 20)
1) With indirect instruction addressing; Address area 0 to 127
2) Plus reaction time of the I/O module (> 1 µs)
3) With direct instruction addressing; Address area 0 to 255
4) I, Q, P, M, L / DB, DI

Load Instructions, continued

If there is a remainder of 3 following an integral division of the used addresses by 4, the execution times for instructions specified on this page are doubled.

Instruction	Address ID	Description	Length in Words	Execution Time in ns		
				CPU 412-3H	CPU 414-4H	CPU 417-4H
L		Load ...				
	IW a	Input word	1[1]/2	75	45	18
	QW	Output word	1[1]/2	75	45	18
	PIW a	Peripheral input word (solo [2])	1[1]/2	75	45	18
		Peripheral-input word (redundant)	1[1]/2	35 µs	24 µs	12 µs
	MW a	Bit memory word	1[3]/2	75	45	18
	LW a	Local data word	2	75	45	18
	DBW a	Data word	2	100	60	24
	DIW a	Instance data word	2	100	60	24
		... into ACCU1-L				
	h [d]	Memory-indirect, area-internal[4]	2	75+/100+	45+/60+	18+/24+
	h [AR1,m]	Register-indirect, area-internal (AR1) [4]	2	75+/100+	45+/60+	18+/24+
	h [AR2,m]	Register-indirect, area-internal (AR2) [4]	2	75+/100+	45+/60+	18+/24+
	W[AR1,m]	Area-crossing (AR1) [4]	2	75+/100+	45+/60+	18+/24+
	W[AR2,m]	Area-crossing (AR2) [4]	2	75+/100+	45+/60+	18+/24+
	Parameter	Via parameter [4]	2	75+/100+	45+/60+	18+/24+

\+ Plus time required for loading the address of the instruction (see page 20)
1) With indirect instruction addressing; Address area 0 to 127
2) Plus reaction time of the I/O module (> 1 µs)
3) With direct instruction addressing; Address area 0 to 255
4) I, Q, P, M, L / DB, DI

Load Instructions, continued

If the used address is divisible by 4without a remainder, the execution times for instructions specified on this page is doubled.

In-struc-tion	Address ID	Description	Length in Words	Execution Time in ns		
				CPU 412-3H	CPU 414-4H	CPU 417-4H
L		Load ...				
	IDa	Input double word	1[1)]/2	75	45	18
	QD a	Output double word	1[1)]/2	75	45	18
	PID a	Peripheral Input double word (solo [2)])	2	75	45	18
		Peripheral-Input double word (redundant)	2	35 µs	24 µs	15 µs
	MD a	Bit memory double word	1[3)]/2	75	45	18
	LD a	Local data double word	2	75	45	18
	DBD a	Data double word	2	100	60	24
	DID a	Instance data double word	2	100	60	24
		... in ACCU1				
	i [d]	Memory-indirect, area internal [4)]	2	75+/100+	45+/60+	18+/24+
	i [AR1,m]	Register-ind., area internal (AR1) [4)]	2	75+/100+	45+/60+	18+/24+
	i [AR2,m]	Register-ind., area internal (AR2) [4)]	2	75+/100+	45+/60+	18+/24+
	D[AR1,m]	Area-crossing (AR1) [4)]	2	75+/100+	45+/60+	18+/24+
	D[AR2,m]	Area-crossing (AR2) [4)]	2	75+/100+	45+/60+	18+/24+
	Parameter	Via parameter [4)]	2	75+/100+	45+/60+	18+/24+

\+ Plus time required for loading the address of the instruction (see page 20)
1) With indirect instruction addressing; Address area 0 to 127
2) Plus reaction time of the I/O module (> 1 µs)
3) With direct instruction addressing; Address area 0 to 255
4) I, Q, P, M, L / DB, DI

Load Instructions, continued

Instruction	Address ID	Description	Length in Words	Execution Time in ns		
				CPU 412-3H	CPU 414-4H	CPU 417-4H
L		Load ...				
	k8	8-bit constant into ACCU1-LL	2	75	45	18
	k16	16-bit constant into ACCU1-L	2	75	45	18
	k32	32-bit constant into ACCU1	3	113	68	27
	Parameter	Load constant into ACCU1 (addressed via parameter)	2	100+	60+	24+
L	2#n	Load 16-bit binary constant into ACCU1-L	2	75	45	18
		Load 32-bit binary constant into ACCU1	3	113	68	27
	B#16#p	Load 8-bit-hexadecimal constant into ACCU1-L	1	75	45	18
L	W#16#p	Load 16-bit hexadecimal constant into ACCU1-L	2	75	45	18
	DW#16#p	Load 32-bit hexadecimal constant into ACCU1	3	113	68	27

Load Instructions, continued

Instruction	Address ID	Description	Length in Words	Execution Time in ns		
				CPU 412-3H	CPU 414-4H	CPU 417-4H
L	'x'	Load 1 character	2	75	45	18
	'xx'	Load 2 characters	2	75	45	18
	'xxx'	Load 3 characters	3	113	68	27
	'xxxx'	Load 4 characters	3	113	68	27
L	D# time value	Load IEC date	3	113	68	27
L	S5T# time value	Load S7 time constant (16 bits)	2	75	45	18
L	TOD# time value	Load IEC time constant	3	113	68	27
L	T# time value	Load 16-bit time constant	2	75	45	18
		Load 32-bit time constant	3	113	68	27
L	C# count value	Load counter constant (BCD code)	2	75	45	18
L	B# (b1, b2)	Load constant as byte (b1, b2)	2	75	45	18
	B# (b1, b2, b3, b4)	Load constant as 4 bytes (b1, b2, b3, b4)	3	113	68	27

Load Instructions, continued

Instruction	Address ID	Description	Length in Words	Execution Time in ns		
				CPU 412-3H	CPU 414-4H	CPU 417-4H
L	P# bit pointer	Load bit pointer	3	113	68	27
L	L# integer	Load 32-bit integer constant	3	113	68	27
L	Real number	Load floating-point number	3	113	68	27

Load Instructions for Timers and Counters

Loading a time value or count value into ACCU1. The contents of ACCU1 are first saved to ACCU2. The bits of the status word are not affected.

Instruction	Address ID	Description	Length in Words	Execution Time in ns		
				CPU 412-3H	CPU 414-4H	CPU 417-4H
L	T f T (e)	Load time value	1[1)]/2 2	75 75+	45 45+	18 18+
	Timer para.	Load time value (addressed via parameter)	2	75+	45+	18+
L	C f C (e)	Load count value	1[1)]/2 2	75 75+	45 45+	18 18+
	Counter para.	Load count value (addressed via parameter)	2	75+	45+	18+
LC	T f T (e)	Load time value in BCD	1[1)]/2 2	75 75+	45 45+	18 18+
	Timer para.	Load time value in BCD (addressed via parameter)	2	75+	45+	18+
LC	C f C (e)	Load count value in BCD	1[1)]/2 2	75 75+	45 45+	18 18+
	Counter para.	Load count value in BCD (addressed via parameter)	2	75+	45+	18+

\+ Plus time required for loading the address of the instruction (see page 20)
1) With direct instruction addressing; Timer/counter No.: 0 to 255

Transfer Instructions

Transferring the contents of ACCU1 to the addressed operand. Note that some instructions are affected by the MCR (see page 95). The status word is not affected.

In-struc-tion	Address ID	Description	Length in Words	Execution Time in ns		
				CPU 412-3H	CPU 414-4H	CPU 417-4H
T		Transfer contents of ACCU1-LL to ...				
	IB a	input byte	1[1]/2	75	45	18
	QB a	output byte	1[1]/2	75	45	18
	PQB a	Peripheral output byte (solo [2])	1[1]/2	75	45	18
		Peripheral-output byte (redundant)	1[1]/2	33 µs	22 µs	12 µs
	MB a	bit memory byte	1[3]/2	75	45	18
	LB a	local data byte	2	75	45	18
	DBB a	data byte	2	100	60	24
	DIB a	instance data byte	2	100	60	24
	g [d]	Memory-indirect, area internal	2	75+/100+	45+/60+	18+/24+
	g [AR1,m]	Register-ind., area internal (AR1)	2	75+/100+	45+/60+	18+/24+
	g [AR2,m]	Register-ind., area internal (AR2)	2	75+/100+	45+/60+	18+/24+
	B[AR1,m]	Area-crossing (AR1)	2	75+/100+	45+/60+	18+/24+
	B[AR2,m]	Area-crossing (AR2)	2	75+/100+	45+/60+	18+/24+
	Parameter	Via parameter	2	75+/100+	45+/60+	18+/24+

\+ Plus time required for loading the address of the instruction (see page 20)
1) With direct instruction addressing; Address area 0 to 127
2) Plus reaction time of the I/O module (> 1 µs)
3) With direct instruction addressing; Address area 0 to 255

Transfer Instructions, continued

If there is a remainder of 3 following an integral division of the used addresses by 4, the execution times for instructions specified on this page are doubled.

Instruction	Address ID	Description	Length in Words	Execution Time in ns		
				CPU 412-3H	CPU 414-4H	CPU 417-4H
T		Transfer contents of ACCU1-L to ...				
		input word	1[1]/2	75	45	18
	IW a	output word	1[1]/2	75	45	18
	QW a	Peripheral input word (solo [2])	1[1]/2	75	45	18
	PQW a	Peripheral-output word (redundant)	1[1]/2	35 µs	24 µs	12 µs
	MW a	bit memory word	1[3]/2	75	45	18
	LW a	local data word	2	75	45	18
	DBW a	data word	2	100	60	24
	DIW a	instance data word	2	100	60	24
	h [d]	Memory-indirect, area internal	2	75+/100+	45+/60+	18+/24+
	h [AR1,m]	Register-ind., area internal (AR1)	2	75+/100+	45+/60+	18+/24+
	h [AR2,m]	Register-ind., area internal (AR2)	2	75+/100+	45+/60+	18+/24+
	W[AR1,m]	Area-crossing (AR1)	2	75+/100+	45+/60+	18+/24+
	W[AR2,m]	Area-crossing (AR2)	2	75+/100+	45+/60+	18+/24+
	Parameter	Via parameter	2	75+/100+	45+/60+	18+/24+

\+ Plus time required for loading the address of the instruction (see page 20)
1) With direct instruction addressing; Address area 0 to 127
2) Plus reaction time of the I/O module (> 1 µs)
3) With direct instruction addressing; Address area 0 to 255

Transfer Instructions, continued

If the used address is divisible by 4without a remainder, the execution times for instructions specified on this page is doubled.

Instruction	Address ID	Description	Length in Words	Execution Time in ns		
				CPU 412-3H	CPU 414-4H	CPU 417-4H
T		Transfer contents of ACCU1 to ...				
	ED a	Input double word	1[1]/2	75	45	18
	AD a	Output double word	1[1]/2	75	45	18
	PAD a	Peripheral output double word (solo [2])	2	75	45	18
		Peripheral-output double word (redundant)	2	35 µs	24 µs	12 µs
	MD a	Bit memory double word	1[3]/2	75	45	18
	LD a	Local data double word	2	75	45	18
	DBD a	Data double word	2	100	60	24
	DID a	Instance data double word	2	100	60	24
T	i [d]	Memory-indirect, area internal	2	75+/100+	45+/60+	18+/24+
	i [AR1,m]	Register-ind., area internal (AR1)	2	75+/100+	45+/60+	18+/24+
	i [AR2,m]	Register-ind., area internal (AR2)	2	75+/100+	45+/60+	18+/24+
	D[AR1,m]	Area-crossing (AR1)	2	75+/100+	45+/60+	18+/24+
	D[AR2,m]	Area-crossing (AR2)	2	75+/100+	45+/60+	18+/24+
	Parameter	Via parameter	2	75+/100+	45+/60+	18+/24+

\+ Plus time required for loading the address of the instruction (see page 20)
1) With direct instruction addressing; Address area 0 to 127
2) Plus reaction time of the I/O module (> 1 µs)
3) With direct instruction addressing; Address area 0 to 255

Load and Transfer Instructions for Address Registers

Loading a double word from a memory area or register into address register 1 (AR1) or address register 2 (AR2). The status word is not affected.

Instruction	Address ID	Description	Length in Words	Execution Time in ns		
				CPU 412-3H	CPU 414-4H	CPU 417-4H
LAR1		Load contents from ...				
	–	ACCU1	1	150	90	36
	AR2	Address register 2	1	150	90	36
	DBD a	Data double word	2	175	105	45
	DID a	Instance data double word	2	175	105	45
	m	32-bit constant as pointer	3	150	90	36
	LD a	Local data double word	2	150	90	36
	MD a	Bit memory double word	2	150	90	36
		... into AR1				
LAR2		Load contents from ...				
	–	ACCU1	1	150	60	36
	DBD a	Data double word	2	175	70	45
	DID a	Instance data double word	2	175	70	45
	m	32-bit constant as pointer	3	150	60	36
	LD a	Local data double word	2	150	60	36
	MD a	Bit memory double word	2	150	60	36
		... into AR2				

Load and Transfer Instructions forAddress Registers, continued

Transferring a double word from address register 1 (AR1) or address register 2 (AR2) to a memory area or register. The contents of ACCU1 are first saved to ACCU2. The status word is not affected.

Instruction	Address ID		Description	Length in Words	Execution Time in ns		
					CPU 412-3H	CPU 414-4H	CPU 417-4H
TAR1			Transfer contents from AR1 in ...				
	–		ACCU1	1	75	45	18
	AR2		Address register 2	1	150	90	36
	DBD	a	Data double word	2	100	60	24
	DID	a	Instance data double word	2	100	60	24
	LD	a	Local data double word	2	75	45	18
	MD	a	Bit memory double word	2	75	45	18
TAR2			Transfer contents from AR2 in ...				
	–		ACCU1	1	75	45	18
	DBD	a	Data double word	2	100	60	24
	DID	a	Instance data double word	2	100	60	24
	LD	a	Local data double word	2	75	45	18
	MD	a	Bit memory double word	2	75	45	18
CAR			Exchange the contents of AR1 and AR2	1	150	90	36

Load and Transfer Instructions for the Status Word

Instruction	Address ID	Description	Length in Words	Execution Time in ns		
				CPU 412-3H	CPU 414-4H	CPU 417-4H
L	STW	Load status word into ACCU1	1	75	45	18

Status word for: **L STW**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Instruction affects:	–	–	–	–	–	–	–	–	–

Instruction	Address ID	Description	Length in Words	Execution Time in ns		
				CPU 412-3H	CPU 414-4H	CPU 417-4H
T	STW	Transfer ACCU1 (bits 0 to 8) to the status word	1	75	45	18

Status word for: **T STW**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

Load Instructions for DB Number and DB Length

Loading the number/length of a data block into ACCU1. The old contents of ACCU1 are saved to ACCU2. The status word is not affected.

Instruction	Address ID	Description	Length in Words	Execution Time in ns		
				CPU 412-3H	CPU 414-4H	CPU 417-4H
L	DBNO	Load number of data block	1	75	45	18
L	DINO	Load number of instance data block	1	75	45	18
L	DBLG	Load length of data block into byte	1	75	45	18
L	DILG	Load length of instance data block into byte	1	75	45	18

Integer Math (16 Bits)

Math instructions on two 16-bit words. The result is written to ACCU1 and/or ACCU1-L. ACCU3 and ACCU4 are then transferred to ACCU2 and ACCU3.

Instruction	Address ID	Description	Length in Words	Execution Time in ns		
				CPU 412-3H	CPU 414-4H	CPU 417-4H
+I		Add 2 integers (16 bits) (ACCU1-L)=(ACCU1-L)+(ACCU2-L)	1	75	45	18
–I		Subtract 1 integer from another (16 bits) (ACCU1-L)=(ACCU2-L)-(ACCU1-L)	1	75	45	18

Status word for: **+I, –I,**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	Yes	Yes	Yes	Yes	–	–	–	–

Integer Math (16 Bits), continued

Instruction	Address ID	Description	Length in Words	Execution Time in ns		
				CPU 412-3H	CPU 414-4H	CPU 417-4H
*I		Multiply 1 integer by another (16 bits) (ACCU1)=(ACCU2-L)*(ACCU1-L)	1	75	45	18
/I		Divide 1 integer by another (16 bits) (ACCU1-L)=(ACCU2-L):(ACCU1-L) The remainder is in ACCU1-H	1	300	180	72

Status word for: ***I, /I**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	Yes	Yes	Yes	Yes	–	–	–	–

Integer Math (32 Bits)

Math instructions on two 32-bit words. The result is written to ACCU1. ACCU3 and ACCU4 are then transferred to ACCU2 and ACCU3.

Instruction	Address ID	Description	Length in Words	Execution Time in ns		
				CPU 412-3H	CPU 414-4H	CPU 417-4H
+D		Add 2 integers (32-bit) (ACCU1)=(ACCU2)+(ACCU1)	1	75	45	18
–D		Subtract 2 integer from another (32 bits) (ACCU1)=(ACCU2)-(ACCU1)	1	75	45	18
*D		Multiply 2 integer by another (32 bits) (ACCU1)=(ACCU2)*(ACCU1)	1	75	45	18

Status word for: **+D, –D,*D, /D**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	Yes	Yes	Yes	Yes	–	–	–	–

Integer Math (32 Bits), continued

Instruction	Address ID	Description	Length in Words	Execution Time in ns		
				CPU 412-3H	CPU 414-4H	CPU 417-4H
/D		Divide 2 integer by another (32 bits) (ACCU1)=(ACCU2):(ACCU1)	1	450	270	108
MOD		Divide 2 integer by another (32 bits) and load the remainder into ACCU1: (ACCU1)=remainder of [(ACCU2):(ACCU1)]	1	450	270	108

Status word for: **/D, MOD**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	Yes	Yes	Yes	Yes	–	–	–	–

Floating-Point Math (32 Bits)

The result of the math instruction is in ACCU1. ACCU3 and ACCU4 are then transferred to ACCU2 and ACCU3.

Instruction	Address ID	Description	Length in Words	Execution Time in ns		
				CPU 412-3H	CPU 414-4H	CPU 417-4H
+R		Add 2 real numbers (32 bits) (ACCU1)=(ACCU2)+(ACCU1)	1	150	90	36
–R		Subtract 1 real number from another (32 bits) (ACCU1)=(ACCU2)-(ACCU1)	1	150	90	36
*R		Multiply 1 real number by another (32 bits) (ACCU1)=(ACCU2)*(ACCU1)	1	150	90	36
/R		Divide 1 real number by another (32 bits) (ACCU1)=(ACCU2):(ACCU1)	1	450	270	108

Status word for: **+R, –R, *R, /R**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	Yes	Yes	Yes	Yes	–	–	–	–

Floating-Point Math (32 Bits), continued

Instruction	Address ID	Description	Length in Words	Execution Time in ns		
				CPU 412-3H	CPU 414-4H	CPU 417-4H
NEGR		Negate the real number in ACCU1	1	75	45	18
ABS		Form the absolute value of the real number in ACCU1	1	75	45	18

Status word for: **NEGR, ABS**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	–	–	–	–	–	–	–	–

Square Root and Square Instructions (32 Bits)

The result of the instruction is in ACCU1. The SQRT instruction can be interrupted.

Instruction	Address ID	Description	Length in Words	Execution Time in ns		
				CPU 412-3H	CPU 414-4H	CPU 417-4H
SQRT		Calculate the square root of a real number in ACCU1	1	600	360	144
SQR		Form the square of the real number in ACCU1	1	150	90	36

Status word for: **SQRT, SQR**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	Yes	Yes	Yes	Yes	–	–	–	–

Logarithmic Function (32 Bits)

The result of the logarithmic function is in ACCU1. The instructions can be interrupted.

Instruction	Address ID	Description	Length in Words	Execution Time in ns		
				CPU 412-3H	CPU 414-4H	CPU 417-4H
LN		Form the natural logarithm of a real number in ACCU1	1	1575	945	378
EXP		Calculate the exponential value of a real number in ACCU1 to the base e (= 2.71828)	1	2400	1440	576

Status word for: **LN, EXP**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	Yes	Yes	Yes	Yes	–	–	–	–

Trigonometrical Functions (32 Bits)

The result of the instruction is in ACCU1. The instructions can be interrupted.

Instruction	Address ID	Description	Length in Words	Execution Time in ns		
				CPU 412-3H	CPU 414-4H	CPU 417-4H
SIN		Calculate the sine of a real number	1	1500	900	360
ASIN		Calculate the arcsine of a real number	1	4875	2925	1170
COS		Calculate the cosine of a real number	1	1500	900	360
ACOS		Calculate the arccosine of a real number	1	4950	2970	1188
TAN		Calculate the tangent of a real number	1	2400	1440	576
ATAN		Calculate the arctangent of a real number	1	1425	855	342

Status word for: **SIN, ASIN, COS, ACOS, TAN, ATAN**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	Yes	Yes	Yes	Yes	–	–	–	–

Adding Constants

Adding integer constants and storing the result in ACCU1. The status word is not affected.

Instruction	Address ID	Description	Length in Words	Execution Time in µs		
				CPU 412-3H	CPU 414-4H	CPU 417-4H
+	i8	Add an 8-bit integer constant	1	75	45	18
+	i16	Add a 16-bit integer constant	2	75	45	18
+	i32	Add a 32-bit integer constant	3	113	68	27

Adding Using Address Registers

Adding a 16-bit integer to the contents of the address register. The value is either specified as an address in the instruction or is in ACCU1-L. The status word is not affected.

Instruction	Address ID	Description	Length in Words	Execution Time in ns		
				CPU 412-3H	CPU 414-4H	CPU 417-4H
+AR1		Add the contents of ACCU1-L to those of AR1	1	150	90	36
+AR1	m (0 to 4095)	Add a pointer constant to the contents of AR1	2	150	90	36
+AR2		Add the contents of ACCU1-L to those of AR2	1	150	90	36
+AR2	m (0 to 4095)	Add pointer constant to the contents of AR2	2	150	90	36

Comparison Instructions (16-Bit Integers)

Comparing the 16-bit integers in ACCU1-L and ACCU2-L. RLO = 1 if the condition is satisfied.

Instruction	Address ID	Description	Length in Words	Execution Time in ns		
				CPU 412-3H	CPU 414-4H	CPU 417-4H
==I		ACCU2-L=ACCU1-L	1	75	45	18
<>I		ACCU2-L≠ACCU1-L	1	75	45	18
<I		ACCU2-L<ACCU1-L	1	75	45	18
<=I		ACCU2-L<=ACCU1-L	1	75	45	18
>I		ACCU2-L>ACCU1-L	1	75	45	18
>=I		ACCU2-L>=ACCU1-L	1	75	45	18

Status word for: **==I, <>I, <I, <=I, >I, >=I**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	Yes	Yes	0	–	0	Yes	Yes	1

Comparison Instructions (32-Bit Integers)

Comparing the 32-bit integers in ACCU1 and ACCU2. RLO = 1 if the condition is satisfied.

Instruction	Address ID	Description	Length in Words	Execution Time in ns		
				CPU 412-3H	CPU 414-4H	CPU 417-4H
==D		ACCU2=ACCU1	1	75	45	18
<>D		ACCU2 ≠ ACCU1	1	75	45	18
<D		ACCU2<ACCU1	1	75	45	18
<=D		ACCU2<=ACCU1	1	75	45	18
>D		ACCU2>ACCU1	1	75	45	18
>=D		ACCU2>=ACCU1	1	75	45	18

Status word for: **==D,< >D, <D, <=D, >D, >=D**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	Yes	Yes	0	–	0	Yes	Yes	1

Comparison Instructions (32-Bit Real Numbers)

Comparing the 32-bit real numbers in ACCU1 and ACCU2. RLO = 1 if the condition is satisfied.

Instruction	Address ID	Description	Length in Words	Execution Time in ns		
				CPU 412-3H	CPU 414-4H	CPU 417-4H
==R		ACCU2=ACCU1	1	75	45	18
<>R		ACCU2 ≠ ACCU1	1	75	45	18
<R		ACCU2<ACCU1	1	75	45	18
<=R		ACCU2<=ACCU1	1	75	45	18
>R		ACCU2>ACCU1	1	75	45	18
>=R		ACCU2>=ACCU1	1	75	45	18

Status word for: **==R, <>R, <R, <=R, >R, >=R**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	Yes	Yes	Yes	Yes	0	Yes	Yes	1

Shift Instructions

Shifting the contents of ACCU1 and ACCU1-L to the left or right by the specified number of places. If no address identifier is specified, the contents of ACCU2-LL are used as the number of places. The last bit shifted is loaded into condition code bit CC 1.

Instruction	Address ID	Description	Length in Words	Execution Time in ns		
				CPU 412-3H	CPU 414-4H	CPU 417-4H
SLW[1)]		Shift the contents of ACCU1-L to the left. Positions that become free are provided with zeros.	1	75	45	18
SLW	0 ... 15					
SLD		Shift the contents of ACCU1 to the left. Positions that become free are provided with zeros.	1	75	45	18
SLD	0 ... 32					
SRW[1)]		Shift the contents of ACCU1-L to the right. Positions that become free are provided with zeros.	1	75	45	18
SRW	0 ... 15					

Status word for: **SLW, SLD, SRW**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	Yes	0	0	–	–	–	–	–

1) No. of places shifted: 0 to 16

Shift Instructions, continued

Instruction	Address ID	Description	Length in Words	Execution Time in ns		
				CPU 412-3H	CPU 414-4H	CPU 417-4H
SRD		Shift the contents of ACCU1 to the right. Positions that become free are provided with zeros.	1	75	45	18
SRD	0 ... 32					
SSI[1)]		Shift the contents of ACCU1-L with sign to the right. Positions that become free are provided with with the sign (bit 15).	1	75	45	18
SSI	0 ... 15					
SSD		Shift the contents of ACCU1 with sign to the right. Positions that become free are provided with with the sign (bit 31).	1	75	45	18
SSD	0 ... 32					

Status word for: **SRD,SSI, SSD**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	Yes	0	0	–	–	–	–	–

1) No. of places shifted: 0 to 16

Rotate Instructions

Rotate the contents of ACCU1 to the left or right by the specified number of places. If no address identifier is specified, the contents of ACCU2-LL are used as the number of places. The last bit shifted is loaded into condition code bit CC1.

Instruction	Address ID	Description	Length in Words	Execution Time in ns		
				CPU 412-3H	CPU 414-4H	CPU 417-4H
RLD		Rotate the contents of ACCU1 to the left	1	75	45	18
RLD	0 ... 32					
RRD		Rotate the contents of ACCU1 to the right	1	75	45	18
RRD	0 ... 32					

Status word for: **RLD, RRD**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	Yes	0	0	–	–	–	–	–

Rotate Instructions, continued

Instruction	Address ID	Description	Length in Words	Execution Time in ns		
				CPU 412-3H	CPU 414-4H	CPU 417-4H
RLDA		Rotate the contents of ACCU1 one bit position to the left through condition code bit CC 1		75	45	18
RRDA		Rotate the contents of ACCU1 one bit position to the right through condition code bit CC 1		75	45	18

Status word for: **RLDA, RRDA**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	Yes	0	0	–	–	–	–	–

Accumulator Transfer Instructions, Incrementing and Decrementing

The status word is not affected.

Instruction	Address ID	Description	Length in Words	Execution Time in ns		
				CPU 412-3H	CPU 414-4H	CPU 417-4H
CAW		Reverse the order of the bytes in ACCU1-L.	1	75	45	18
CAD		Reverse the order of the bytes in ACCU1.	1	75	45	18
TAK		Swap the contents of ACCU1 and ACCU2	1	75	45	18
ENT		The contents of ACCU2 and ACCU3 are transferred to ACCU3 and ACCU4.	1	75	45	18
LEAVE		The contents of ACCU3 and ACCU4 are transferred to ACCU2 and ACCU3.	1	75	45	18
PUSH		The contents of ACCU1, ACCU2 and ACCU3 are transferred to ACCU2, ACCU3 and ACCU4	1	75	45	18
POP		The contents of ACCU2, ACCU3 and ACCU4 are transferred to ACCU1, ACCU2 and ACCU3	1	75	45	18
INC	k8	Increment ACCU1-LL	1	75	45	18
DEC	k8	Decrement ACCU1-LL	1	75	45	18

Program Display and Null Operation Instructions

The status word is not affected.

Instruction	Address ID	Description	Length in Words	Execution Time in ns		
				CPU 412-3H	CPU 414-4H	CPU 417-4H
BLD	k8	Program display instruction: Is treated by the CPU as a null operation instruction.	1	38	23	9
NOP	0 1	Null operation instruction	1	38	23	9

Data Type Conversion Instructions

The results of the conversion are in ACCU1.

Instruction	Addr. ID	Description	Length in Words	Execution Time in in ns		
				CPU 412-3H	CPU 414-4H	CPU 417-4H
BTI		Convert contents of ACCU1-L from BCD (0 to +/- 999) to integer (16 bits) (**B**CD **T**o **I**nt)	1	75	45	18
BTD		Convert contents of ACCU1 from BCD (0 to +/-9 999 999) to double integer (32 bits) (**B**CD **T**o **D**oubleint)	1	75	45	18
DTR		Convert contents of ACCU1 from double integer (32 bits) to real number (32 bits) (**D**oubleint **T**o **R**eal)	1	150	90	36
ITD		Convert contents of ACCU1 from integer (16 bits) to double integer (32 bits) (**I**nt **T**o **D**oubleint)	1	75	45	18

Status word for: **BTI, BTD, DTR, ITD**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	–	–	–	–	–	–	–	–

Data Type Conversion Instructions, continued

Instruction	Addr. ID	Description	Length in Words	Execution Time in ns		
				CPU 412-3H	CPU 414-4H	CPU 417-4H
ITB		Convert contents of ACCU1-L from integer (16 bits) to BCD from 0 to +/- 999 (**I**nt **T**o **B**CD)	1	75	45	18
DTB		Convert contents of ACCU1 from double integer (32 bits) to BCD from 0 to +/- 9 999 999 (**D**oubleint **T**o **B**CD)	1	75	45	18

Status word for: **ITB, DTB**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	–	–	Yes	Yes	–	–	–	–

Data Type Conversion Instructions, continued

The real number to be converted is in ACCU1.

Instruction	Address ID	Description	Length in Words	Execution Time in ns		
				CPU 412-3H	CPU 414-4H	CPU 417-4H
RND+		Convert a real number into a 32-bit integer. The number is rounded up to the next whole number.	1	75	45	18
RND		Convert a real number into a 32-bit integer.	1	75	45	18
RND-		Convert a real number into a 32-bit integer. The number is rounded down to the next whole number.	1	75	45	18
TRUNC		Convert a real number into a 32-bit integer. The places after the decimal point are truncated.	1	75	45	18

Status word for: **RND, RND-, RND+, TRUNC**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	–	–	Yes	Yes	–	–	–	–

Forming the Ones and Twos Complements

Instruction	Address ID	Description	Length in Words	Execution Time in ns		
				CPU 412-3H	CPU 414-4H	CPU 417-4H
INVI		Form the ones complement of ACCU1-L	1	75	45	18
INVD		Form the ones complement of ACCU1	1	75	45	18

Status word for: **INVI, INVD**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	–	–	–	–	–	–	–	–

NEGI		Form the twos complement of ACCU1-L (integer)	1	75	45	18
NEGD		Form the twos complement of ACCU1 (double integer)	1	75	45	18

Status word for: **NEGI, NEGD**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	Yes	Yes	Yes	Yes	–	–	–	–

Block Call Instructions

The runtimes of the System Functions are specified in the chapter entitled “System Functions” as of page 104.

The information on the status word only relates to the block call itself and not to the commands called in this block.

In-struc-tion	Address ID	Description	Length in Words	Execution Time in ns		
				CPU 412-3H	CPU 414-4H	CPU 417-4H
CALL	FB q, DB q	Unconditional call of an FB, with parameter transfer	15/17[1)]	2425 [2)]	1455 [2)]	528 [2)]
CALL	SFB q, DB q	Unconditional call of an SFB, with parameter transfer	16/17[1)]	2425 [2)]	1455 [2)]	528 [2)]
CALL	FC q	Unconditional call of a function, with parameter transfer	7/8[1)]	2100 [2)]	11260 [2)]	456 [2)]
CALL	SFC q	Unconditional call of an SFC, with parameter transfer	8	2100 [2)]	1260 [2)]	456 [2)]

Status word for: **CALL**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	–	–	–	0	0	1	–	0

1) The instruction length depends on the block number from (0...255 or more)
2) Plus time required for supplying parameters

Block Call Instructions, continued

In-struc-tion	Address ID	Description	Length in Words	Execution Time in ns CPU 412-3H	CPU 414-4H	CPU 417-4H
UC	FB q	Unconditional call of blocks,	1[1]/2	1450	870	294
	FC q	without parameter transfer		1450	870	294
	FB [e]	Memory-indirect FB call	2	1450+	870+	294+
	FC [e]	Memory-indirect FC call	2	1450+	870+	294+
	Parameter	FB/FC call via parameter	2	1450+	870+	294+
CC	FB q	Conditional call of blocks, without	1[1]/2	1600/325 [3]	960/195 [3]	330/78 [3]
	FC q	parameter transfer		1600/325 [3]	960/195 [3]	330/78 [3]
	FB [e]	Memory-indirect FB call	2	1600+/325+ [3]	960+/195+ [3]	330+/78+ [3]
	FC [e]	Memory-indirect FC call	2	1600+/325+ [3]	960+/195+ [3]	330+/78+ [3]
	Parameter	FB/FC call via parameter	2	1600+/325+ [3]	960+/195+ [3]	330+/78+ [3]

Status word for: **UC, CC [2]**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	–	–	–	0	0	1	–	0

\+ Plus time required for loading the address of the instruction (see page 20)
1) With direct instruction (DB) addressing; Block No. 0 to 255
2) Depending on RLO, sets RLO = 1
3) If call is not executed

Block Call Instructions, continued

Instruction	Address ID	Description	Length in Words	Execution Time in ns					
				CPU 412-3H		CPU 414-4H		CPU 417-4H	
				1. open	2. - n. open [1]	1. open	2. - n. open [1]	1. open	2. - n. open [1]
OPN		Select a data block							
	DB q DI q	Direct data block, DB Direct instance DB	2	300	75	180	45	72	18
	DB [e] DI [e]	Data block, indirect save Bit memory area M Local data area L Data block DB/DI	2	 450 450 475	 225 225 250	 270 270 295	 135 135 150	 108 108 114	 54 54 60
OPN	Param.	Data block via parameters	2	475	250	295	150	114	60

Status word for: **OPN**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	–	–	–	–	–	–	–	–

[1] if the same DB or DI is already selected

Block End Instructions

Instruction	Address ID	Description	Length in Words	Execution Time in ns		
				CPU 412-3H	CPU 414-4H	CPU 417-4H
BE		End block	1	1750	1050	420
BEU		End block unconditionally	1	1750	1050	420

Status word for: **BE, BEU**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	–	–	–	0	0	1	–	0

BEC		End block conditionally if RLO = “1”		1900 325 [1]	1140 195 [1]	456 78 [1]

Status word for: **BEC**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	Yes	–
Instruction affects:	–	–	–	–	Yes	0	1	1	0

[1] If jump is not executed

Exchanging Shared Data Block and Instance Data Block

Exchanging the two current data blocks. The current shared data block becomes the current instance data block, and vice versa. The status word is not affected.

Instruction	Address ID	Description	Length in Words	Execution Time in ns		
				CPU 412-3H	CPU 414-4H	CPU 417-4H
CDB		Exchange shared data block and instance data block	1	150	90	36

Jump Instructions

Jumping as a function of conditions.

Instruction	Address ID	Description	Length in Words	Execution Time in ns		
				CPU 412-3H	CPU 414-4H	CPU 417-4H
JU	LABEL	Jump unconditionally	2	500	300	126

Status word for: **JU**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	–	–	–	–	–	–	–	–

JC	LABEL	Jump if RLO = “1”	2	500/75 [1]	300/45 [1]	126/18 [1]
JCN	LABEL	Jump if RLO = “0”	2	500/75 [1]	300/45 [1]	126/18 [1]

Status word for: **JC, JCN**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	Yes	–
Instruction affects:	–	–	–	–	–	0	1	1	0

[1] If jump is not executed

Jump Instructions, continued

Instruction	Address ID	Description	Length in Words	Execution Time in ns		
				CPU 412-3H	CPU 414-4H	CPU 417-4H
JCB	LABEL	Jump if RLO = “1”. Save the RLO in the BR bit	2	500/75 [1]	300/45 [1]	126/18 [1]
JNB	LABEL	Jump if RLO = “0”. Save the RLO in the BR bit	2	500/75 [1]	300/45 [1]	126/18 [1]

Status word for: **JCB, JNB**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	Yes	–
Instruction affects:	Yes	–	–	–	–	0	1	1	0

JBI	LABEL	Jump if BR = “1”	2	500/75 [1]	300/45 [1]	126/18 [1]
JNBI	LABEL	Jump if BR = “0”	2	500/75 [1]	300/45 [1]	126/18 [1]

Status word for: **JBI, JNBI**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	Yes	–	–	–	–	–	–	–	–
Instruction affects:	–	–	–	–	–	0	1	–	0

[1] If jump is not executed

Jump Instructions, continued

Instruction	Address ID	Description	Length in Words	Execution Time in ns		
				CPU 412-3H	CPU 414-4H	CPU 417-4H
JO	LABEL	Jump on stored overflow (OV = “1”)	2	500/75 [1]	300/45 [1]	126/18 [1]

Status word for: **JO**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	Yes	–	–	–	–	–
Instruction affects:	–	–	–	–	–	–	–	–	–

JOS	LABEL	Jump on stored overflow (OS = “1”)	2	500/75 [1]	300/45 [1]	126/18 [1]

Status word for: **JOS**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	Yes	–	–	–	–
Instruction affects:	–	–	–	–	0	–	–	–	–

[1] If jump is not executed

Jump Instructions, continued

Instruction	Address ID	Description	Length in Words	Execution Time in ns		
				CPU 412-3H	CPU 414-4H	CPU 417-4H
JUO	LABEL	Jump if “unordered math instruction” (CC1=1 and CC0=1)	2	500/75 [1]	300/45 [1]	126/18 [1]
JZ	LABEL	Jump if result = 0 (CC1=0 and CC0=0)	2	500/75 [1]	300/45 [1]	126/18 [1]
JP	LABEL	Jump if result > 0 (CC1=1 and CC0=0)	2	500/75 [1]	300/45 [1]	126/18 [1]
JM	LABEL	Jump if result < 0 (CC1=0 and CC0=1)	2	500/75 [1]	300/45 [1]	126/18 [1]
JN	LABEL	Jump if result ≠ 0 (CC1=1 and CC0=0) or (CC1=0 and CC0=1)	2	500/75 [1]	300/45 [1]	126/18 [1]

Status word for: **JUO, JZ, JP, JM, JN,**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	Yes	Yes	–	–	–	–	–	–
Instruction affects:	–	–	–	–	–	–	–	–	–

[1] If jump is not executed

Instruction	Address ID	Description	Length in Words	Execution Time in ns		
				CPU 412-3H	CPU 414-4H	CPU 417-4H
JMZ	LABEL	Jump if result ≤ 0 (CC1=0 and CC0=1) or (CC1=0 and CC0=0)	2	500/75 [1)]	300/45 [1)]	126/18 [1)]
JPZ	LABEL	Jump if result ≥ 0 (CC1=1 and CC0=0) or (CC1=0 and CC0=0)	2	500/75 [1)]	300/45 [1)]	126/18 [1)]

Status word for: **JUO, JZ, JP, JM, JN, JMZ, JPZ**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	Yes	Yes	–	–	–	–	–	–
Instruction affects:	–	–	–	–	–	–	–	–	–

[1)] If jump is not executed

Jump Instructions, continued

Instruction	Address ID	Description	Length in Words	Execution Time in ns		
				CPU 412-3H	CPU 414-4H	CPU 417-4H
JL	LABEL	Jump distributor This instruction is followed by a list of jump instructions. The address identifier is a jump label to subsequent instructions in this list. ACCU1-LL contains the number of the jump instruction to be executed (max. 254). The number of the first jump instruction is 0.	2	575	345	144
LOOP	LABEL	Decrement ACCU1-L and jump if ACCU1-L ≠ 0 (loop programming)	2	400/75 [1]	240/45 [1]	96/18 [1]

Status word for: **JL, LOOP**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	–	–	–	–	–	–	–	–

[1] If jump is not executed

Instructions for the Master Control Relay (MCR)

MCR=1→MCR is deactivated
MCR=0→MCR is activated; “T” and “=” instructions write zeros to the

corresponding address identifiers if RLO = “0”; “S” and ”R” instructions leave the memory contents unchanged.

Instruction	Address ID	Description	Length in Words	Execution Time in ns		
				CPU 412-3H	CPU 414-4H	CPU 417-4H
MCR(		Open an MCR zone. Save the RLO to the MCR stack.	1	75	45	18

Status word for: **MCR(**	CC1	BR	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	Yes	–
Instruction affects:	–	–	–	–	–	0	1	–	0

)MCR		Close an MCR zone. Pop an entry off the MCR stack.	1	75	45	18

Status word for: **)MCR**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	–	–	–	–	0	1	–	0

Instructions for the Master Control Relay (MCR), continued

Instruction	Address ID	Description	Length in Words	Execution Time in ns		
				CPU 412-3H	CPU 414-4H	CPU 417-4H
MCRA		Activate the MCR	1	75	45	18
MCRD		Deactivate the MCR	1	75	45	18

Status word for: **MCRA, MCRD**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction evaluates:	–	–	–	–	–	–	–	–	–
Instruction affects:	–	–	–	–	–	–	–	–	–

Oganization Blocks (OB)

A user program for the S7-400 is made up of blocks containing the statements, parameters and data for the relevant CPU. The number of blocks you can create or which are provided by the operating system is different for each of the S7-400 CPUs. You will find a detailed description of the OBs and their use in the manual *Programming with STEP 7*.

Organization Blocks	CPU 412-3H	CPU 414-4H	CPU 417-4H	Start Events (Hexadecimal Values)
Free cycle				
OB 1	x	x	x	1101, 1102, 1103, 1104, 1105
Time-of-day interrupts				
OB 10	x	x	x	1111
OB 11	x	x	x	1112
OB 12	x	x	x	1113
OB 13	x	x	x	1114
OB 14			x	1115
OB 15			x	1116
OB 16			x	1117
OB 17			x	1118

Oganization Blocks (OB), continued

Organization Blocks	CPU 412-3H	CPU 414-4H	CPU 417-4H	Start Events (Hexadecimal Values)
Time-delay interrupts				
OB 20	x	x	x	1121
OB 21	x	x	x	1122
OB 22	x	x	x	1123
OB 23	x	x	x	1124
Timed interrupts [1]				
OB 30			x	1131
OB 31			x	1132
OB 32	x	x	x	1133
OB 33	x	x	x	1134
OB 34	x	x	x	1135
OB 35	x	x	x	1136
OB 36			x	1137
OB 37			x	1138
OB 38			x	1139

[1] Further start events of H-CPUs for OB 30 to OB 38: 1130_H

Organization Blocks (OB), continued

Organization Blocks	CPU 412-3H	CPU 414-4H	CPU 417-4H	Start Events (Hexadecimal Values)
Hardware interrupts				
OB 40	x	x	x	1141, 1142, 1143, 1144, 1145
OB 41	x	x	x	1141, 1142, 1143, 1144, 1145
OB 42	x	x	x	1141, 1142, 1143, 1144, 1145
OB 43	x	x	x	1141, 1142, 1143, 1144, 1145
OB 44			x	1141, 1142, 1143, 1144, 1145
OB 45			x	1141, 1142, 1143, 1144, 1145
OB 46			x	1141, 1142, 1143, 1144, 1145
OB 47			x	1141, 1142, 1143, 1144, 1145
Interrupt OBs for DPV1:				
OB 55	x	x	x	1155
OB 56	x	x	x	1156
OB 57	x	x	x	1157

Oganization Blocks (OB), continued

Organization Blocks	CPU 412-3H	CPU 414-4H	CPU 417-4H	Start Events (Hexadecimal Values)
Redundancy error interrupts:				
OB 70	x	x	x	73A2, 73A3, 72A3
OB 72	x	x	x	7301, 7302, 7303, 7320, 7321, 7322, 7323, 7331, 7333, 7334, 7335, 7340, 7341, 7342, 7343, 7344, 7950, 7951, 7952, 7852, 7953, 7954, 7955, 7855, 7956, 73C1, 73C2
Asynchronous error interrupts:				
OB 80	x	x	x	3501, 3502, 3505, 3506, 3507, 350A
OB 81	x	x	x	3821, 3822, 3823, 3825, 3826, 3827, 3831, 3832, 3833, 3921, 3922, 3923, 3925, 3926, 3927, 3931, 3932, 3933
OB 82	x	x	x	3842, 3942
OB 83	x	x	x	3267, 3367, 3861, 3863, 3864, 3865, 3961, 3968

Oganization Blocks (OB), continued

Organization Blocks	CPU 412-3H	CPU 414-4H	CPU 417-4H	Start Events (Hexadecimal Values)
OB 84	x	x	x	3582, 3583, 3986, 3587
OB 85	x	x	x	35A1, 35A2, 35A3, 38B3, 38B4, 39B1, 39B2, 39B3, 39B4
OB 86	x	x	x	38C1, 38C2, 39C1, 38C6, 38C7, 38C8 38C4[1)], 38C5[1)], 39C3[1)], 39C4[1)], 39C5[1)]
OB 87	x	x	x	35D2, 35D3, 35D4, 35D5, 35E1, 35E2, 35E3, 35E4, 35E5, 35E6
OB 88	x	x	x	3571, 3572, 3573, 3574, 3575, 3576, 3578, 357A
Warm restart:				
OB 100	x	x	x	1381, 1382, 138A, 138B
Cold restart:				
OB 102	x	x	x	1385, 1386, 1387, 1388
Synchronous error interrupts:				
OB 121	x	x	x	2521, 2522, 2523, 2524, 2525, 2526, 2527, 2528, 2529, 2530, 2531, 2532, 2533, 2534, 2535, 253A, 253C, 253D, 253E, 253F
OB 122	x	x	x	2942, 2943, 2944, 2945

Function Blocks (FB)

The following tables list the quantities, numbers and maximum sizes of the function blocks you can create for the various S7-400 CPUs.

Function Blocks	CPU 412–3H	CPU 414	CPU 417
Quantity	2048	2048	6144
Permissible numbers	0 to 2047	0 to 2047	0 to 6143
Maximum size of a function block (code required for execution)	64 KByte	64 KByte	64 KByte

Functions (FC) and Data Blocks

The following tables list the quantities, numbers and maximum sizes of the functions and data blocks you can create for the various S7-400 CPUs.

Functions	CPU 412–3H	CPU 414	CPU 417
Quantity	2048	2048	6144
Permissible numbers	0 to 2047	0 to 2047	0 to 6143
Maximum size of a function (code required for execution)	64 KByte	64 KByte	64 KByte

Data Blocks	CPU 412–3H	CPU 414	CPU 417
Quantity	4095	4095	4095
Permissible numbers	1 to 4095	1 to 4095	1 to 4095
Maximum size of a data block (number of data bytes)	64 KByte	64 KByte	64 KByte

System Functions

The following tables show the system functions which are provided by the operating system of the S7-400 CPUs and the execution times for the various CPUs. (X: function available, execution times not yet available before printing).

SFC No.	SFC Name	Function	Execution Time in µs					
			CPU 412-3H solo	CPU 412-3H redun-dant	CPU 414-4H solo	CPU 414-4H redun-dant	CPU 417-4H solo	CPU 417-4H redun-dant
0	SET_CLK	Set clock	291	618	184	375	78	161
1	READ_CLK	Read clock	21	60	13	38	5	18
2	SET_RTM	Set run-time meter	18	18	11	11	4	4
3	CTRL_RTM	Start and stop run-time meter	14	14	9	9	4	4
4	READ_RTM	Read run-time meter	20	56	12	36	5	13
5	GADR_LGC	Find logical address of a channel Rack 0	26	26	16	16	7	7
		internal DP	32	32	20	20	8	8
6	RD_SINFO	Read start information of current OB	23	23	15	15	6	6
9	EN_MSG	Enable block-related, symbol-related, and group status messages. First call, REQ = 1	105	179	65	112	37	51
		Last call	27	65	17	41	9	21

SFC No.	SFC Name	Function	Execution Time in µs					
			CPU 412-3H solo	CPU 412-3H redun-dant	CPU 414-4H solo	CPU 414-4H redun-dant	CPU 417-4H solo	CPU 417-4H redun-dant
10	DIS_MSG	Disable block-related, symbol-related, and group status messages. First call, REQ = 1	105	178	65	112	37	51
		Last call	28	65	17	42	9	21
13	DP_NRMDG	Read slave diagnostic data First call	151	200	95	129	47	85
		Intermediate call	63	63	39	39	19	19
		Last call (28 bytes)	83	83	73	73	24	24
14	DPRD_DAT	Read consistent user data (n bytes) via integrated DP interface 3 bytes	49	93	31	59	14	24
		via integrated DP interface 32 bytes	50	109	33	70	14	30
		via external DP interface 3 bytes	83	93	52	65	15	31
		via external DP interface 32 bytes	162	217	101	171	55	68

SFC No.	SFC Name	Function	Execution Time in µs					
			CPU 412-3H solo	CPU 412-3H redun-dant	CPU 414-4H solo	CPU 414-4H redun-dant	CPU 417-4H solo	CPU 417-4H redun-dant
15	DPWR_DAT	Write consistent user data (n bytes) via integrated DP interface 3 bytes	49[1)] 57[2)]	86[1)] 91[2)]	31[1)] 33[2)]	54[1)] 58[2)]	12[1)] 13[2)]	21[1)] 24[2)]
		via integrated DP interface 32 bytes	52[1)] 58[2)]	89[1)] 95[2)]	32[1)] 34[2)]	56[1)] 62[2)]	13[1)] 14[2)]	24[1)] 26[2)]
		via external DP interface 3 bytes	85[1)] 93[2)]	99[1)] 105[2)]	52[1)] 56[2)]	60[1)] 62[2)]	18[1)] 20[2)]	25[1)] 26[2)]
		via external DP interface 32 bytes	186[1)] 215[2)]	193[1)] 223[2)]	114[1)] 128[2)]	120[1)] 133[2)]	75[1)] 79[2)]	89[1)] 100[2)]
17	ALARM_SQ	Generate acknowledgeable block-related messages. First call, SIG = 0 –> 1	259-587 3)	574-941 3)	160-371 3)	383-588 3)	67-234 3)	162-334 3)
		Empty call	71-388 3)	165-477 3)	50-246 3)	106-308 3)	17-182 3)	46-215 3)
18	ALARM_S	Generate unacknowledgeable block-related messages. First call, SIG = 0 –> 1	265-595 3)	607-940 3)	169-376 3)	377-580 3)	65-238[3)]	161-330 3)
		Empty call	66-392 3)	161-471 3)	46-249 3)	106-300 3)	17-185 3)	45-210 3)
19	ALARM_SC	Acknowledgment status of the last ALARM_SQ entering state message.	59-378 3)	177-487 3)	40-256 3)	92-310 3)	16-187 3)	42-208 3)

1) without data transmission to the process image

2) with data transmission to the process image

3) Depending on the number of active messages (assigned system resources)

SFC No.	SFC Name	Function	Execution Time in µs					
			CPU 412-3H solo	CPU 412-3H redun-dant	CPU 414-4H solo	CPU 414-4H redun-dant	CPU 417-4H solo	CPU 417-4H redun-dant
20	BLKMOV	Copy variable within the work memory (n = number of bytes to be copied)	38 + n * 0,052	38 + n * 0,052	22 + n * 0,036	22 + n * 0,036	8 + n * 0,016	8 + n * 0,016
		Source = Load memory	477 + n * 1,3	1212 + n * 2,2	520 + n * 1,2	1042 + n * 1,2	378 + n * 0,8	713 + n * 0,8
21	FILL	Set array default variables within the work memory (n = length of target variables in bytes)	31 + n * 0,025	31 + n * 0,025	20 + n * 0,016	20 + n * 0,016	7 + n * 0,01	7 + n * 0,01
22	CREAT_DB	Create data block n = DB length [bytes]	102 + n * 0,06	290 + n * 0,06	64 + n * 0,04	192 + n * 0,04	27 + n * 0,02	84 + n * 0,02
		Occupy last free DB No. from a field of 100 DBs	612	801	387	514	156	214
23	DEL_DB	Delete data block	134	620	84	403	34	182
24	TEST_DB	Test data block	47	231	29	148	12	70
25	COM-PRESS	Compress user memory First call (trigger)	79	164	50	105	21	47
		Intermediate call (active)	13	13	8	8	3	3

SFC No.	SFC Name	Function	Execution Time in µs					
			CPU 412-3H solo	CPU 412-3H redundant	CPU 414-4H solo	CPU 414-4H redundant	CPU 417-4H solo	CPU 417-4H redundant
26	UPDAT_PI	Update process image input table (run-time entry for 1 DI 32 in the central rack)	29	54	21	37	12	18
		AI 8* 13Bit	51	151	41	106	31	61
27	UPDAT_PO	Update process image output table (run-time entry for 1 DO 32 in the central rack)	28	53	20	35	12	17
		AO 8* 13Bit	48	149	38	104	29	58
28	SET_TINT	Set time-of-day interrupt	57	99	35	61	15	28
29	CAN_TINT	Cancel time-of-day interrupt	121	460	79	300	34	134
30	ACT_TINT	Activate time-of-day interrupt	37	77	23	49	9	22
31	QRY_TINT	Query time-of-day interrupt	11	11	7	7	3	3
32	SRT_DINT	Start time-delay interrupt	33	33	17	17	7	7
33	CAN_DINT	Cancel time-delay interrupt	25	25	16	16	6	6
34	QRY_DINT	Query time-delay interrupt	12	12	7	7	3	3
36	MSK_FLT	Mask synchronous faults	14	14	9	9	4	4
37	DMSK_FLT	Demask synchronous faults	16	16	10	10	4	4
38	READ_ERR	Read error register	16	16	9	9	4	4

SFC No.	SFC Name	Function	Execution Time in µs					
			CPU 412-3H solo	CPU 412-3H redun-dant	CPU 414-4H solo	CPU 414-4H redun-dant	CPU 417-4H solo	CPU 417-4H redun-dant
39	DIS_IRT	Discard new events Block all events (MODE = 0)	113	113	71	71	29	29
		Block all events of a priority class (MODE = 1)	28	28	18	18	7	7
		Block one event (MODE = 2)	17	17	11	11	4	4
40	EN_IRT	Stop discarding events Enable all events (MODE = 0)	108	108	67	67	27	27
		Enable all events in a priority class (MODE = 1)	27	27	17	17	6	6
		Enable an event (MODE = 2)	16	16	10	10	4	4
41	DIS_AIRT	Delay interrupt events the first time delay is activated[1)]	130	130	81	81	34	34
		if the delay is already activated	10	10	6	6	2	2

[1)] When activating the delay for the first time, the SFC 41 runtime depends on the priority class in which the SFC 41 is called. The specified runtime refers to the call in OB 1. It decreases while the priority class number increases.

SFC No.	SFC Name	Function	Execution Time in µs					
			CPU 412-3H solo	CPU 412-3H redun-dant	CPU 414-4H solo	CPU 414-4H redun-dant	CPU 417-4H solo	CPU 417-4H redun-dant
42	EN_AIRT	if other delays are present	12	12	8	8	3	3
		Stop delaying interrupt eventswhen can-celing the last delay 1)	240	240	150	150	66	66
43	RE_TRIGR	Retrigger watchdog monitoring	115	395	72	259	31	116
44	REPL_VAL	Transfer substitute value to ACCU1	14	14	8	8	3	3
46	STP	Force CPU into STOP mode cannot be measured	--	--	--	--	--	--
47	WAIT	Delay program execution in addition to waiting time	10	10	7	7	3	3
48	SNC_RTCB	Synchronize slave clocks	13	48	8	31	3	14
49	LGC_GADR	Find slot with logical address	28	28	17	17	7	7
50	RD_LGADR	Find all logical addresses of a block (run-time entry for 1 DI 32 in the central rack)	67	67	42	42	17	17

1) When cancelling the last delay, the SFC 42 runtime depends on the priority class in which the SFC 42 is called. The specified runtime refers to the call in OB 1. It decreases while the priority class number increases.

SFC-No.	SFC-Name	Function	Execution Time in µs					
			CPU 412-3H solo	CPU 412-3H redun-dant	CPU 414-4H solo	CPU 414-4H redun-dant	CPU 417-4H solo	CPU 417-4H redun-dant
51	RDSYSST	“Module identification” partial list Display one data record (0111)	87	87	54	54	22	23
51	RDSYSST	”Module Identification” partial list Display all data records (0012)	161	161	100	100	41	42
		Display one data record (0112)	103	103	64	64	27	27
		Display header information (0F12)	75	75	46	46	19	19
51	RDSYSST	“Save” partial list Display header information (0113)	96	96	59	59	25	25

SFC-No.	SFC-Name	Function	Execution Time in µs					
			CPU 412-3H solo	CPU 412-3H redun-dant	CPU 414-4H solo	CPU 414-4H redun-dant	CPU 417-4H solo	CPU 417-4H redun-dant
51	RDSYSST	"System Areas" partial list Display all data records (0014)	102	102	63	63	26	26
		Display header information (0F14)	74	74	46	46	19	19
51	RDSYSST	"Block Types" partial list Display all data records (0015)	93	93	57	57	24	24
51	RDSYSST	"Status of Module LEDs" partial list Display status of all LEDs (0019)	182	--	125	--	59	--
		Display header information (0F19)	126	--	79	--	32	--
51	RDSYSST	"Component Identification" partial list Display all components (001C)	133	338	83	221	34	107
		Display one of the components (011C)	98	300	61	196	25	98
		Display all components of a H–system CPU (021C)	134	337	84	220	35	107
		Display a component of all redundant CPUs of the H-system (031C)	99	317	61	207	26	103
		Display header information (0F1C)	82	284	51	186	21	94
51	RDSYSST	"Interrupt status" partial list Display one data record (0222)	113	113	70	70	29	29

SFC-No.	SFC-Name	Function	Execution Time in µs					
			CPU 412-3H solo	CPU 412-3H redun-dant	CPU 414-4H solo	CPU 414-4H redun-dant	CPU 417-4H solo	CPU 417-4H redun-dant
51	RDSYSST	“TPA /CPU assignment” partial list Assignment between all process image partitions and OBs (0025)	221	221	138	138	56	56
		Assignment between a process image partition and the corresponding OB (0125)	89	89	55	55	23	23
51	RDSYSST	“Status information communication” partial list Display status information of a communication unit (0132)	111 - 182	139 - 577	69 - 113	87 - 374	29 - 47	40 - 166
51	RDSYSST	“Status information communication” partial list Display status information of a communication unit (0232)	156	311	97	201	41	90
51	RDSYSST	“H-CPU group information” partial list Current status of the H system (0071)	-	122	-	84	-	36
		Header information (0F71)	-	69	-	42	-	18
51	RDSYSST	“Modules LEDs” partial list Status of an LED (0174)	136	167	86	106	36	47

SFC-No.	SFC-Name	Function	Execution Time in µs					
			CPU 412-3H solo	CPU 412-3H redun-dant	CPU 414-4H solo	CPU 414-4H redun-dant	CPU 417-4H solo	CPU 417-4H redun-dant
51	RDSYSST	“Switched DP slaves in the H system” partial list Communication status between the H system and a switched DP slave (0C75)	-	133	-	82	-	53
51	RDSYSST	“DP master system information” partial list All known DP master systems of the CPU (0090)	225	225	140	140	57	57
		A DP-Mastersystem (0190)	91	91	56	56	23	23
		Header information (0F90)	76	76	47	47	20	20
51	RDSYSST	“Module status information” partial list central a module with logical basic address (0C91)	134	221	83	141	35	79
		dezentral a module with logical basic address (0C91)	164	254	103	167	43	98

SFC-No.	SFC-Name	Function	Execution Time in µs					
			CPU 412-3H solo	CPU 412-3H redun-dant	CPU 414-4H solo	CPU 414-4H redun-dant	CPU 417-4H solo	CPU 417-4H redun-dant
51	RDSYSST	"Module status information" partial listof a module (distributed) with logical basic address (4C91) First call	186	266	116	170	49	76
		"Module status information" partial listof a module (distributed) with logical basic address (4C91) Intermediate call	118	118	74	74	31	31
		"Module status information" partial list of a module (distributed) with logical basic address (4C91) Last call	138	138	80	80	33	33
51	RDSYSST	Central all modules in the specified rack (n=number DR) (0D91)	188 + n* 18	320 + n* 20	118 + n * 14	211 + n * 14	49 + n * 10	91 + n * 12
		Distributed all modules in the specified DP station (0D91)	154 - 178	288 - 331	95 – 108	188 - 209	38 - 45	84 - 94

SFC-No.	SFC-Name	Function	Execution Time in µs					
			CPU 412-3H solo	CPU 412-3H redun-dant	CPU 414-4H solo	CPU 414-4H redun-dant	CPU 417-4H solo	CPU 417-4H redun-dant
51	RDSYSST	"Rack/station status information" partial list central Display setpoint status of rack 0 (0092)	96	125	59	79	25	37
		distributed Display setpoint status of DP system 1 (0092)	376	420	235	263	95	108
51	RDSYSST	Display the actual status of the stations of a DP master system (via external DP interface) (4292)	163	239	102	150	43	68
51	RDSYSST	Display activation status of DP master system 1 (via integrated DP interface) (0192)	453	478	284	312	125	136
51	RDSYSST	central Display the actual status of rack 0 (0292)	96	125	60	79	25	37
		distributed Display the actual status of DP system 1 (0292)	393	434	245	272	100	112

SFC-No.	SFC-Name	Function	Execution Time in µs					
			CPU 412-3H solo	CPU 412-3H redun-dant	CPU 414-4H solo	CPU 414-4H redun-dant	CPU 417-4H solo	CPU 417-4H redun-dant
51	RDSYSST	Display the actual status of the stations of a DP master system (via external DP interface) (4292)	163	237	102	151	42	68
51	RDSYSST	Display the status of rack 0 battery buffer if at least one battery has failed (0392)	96	124	59	78	25	37
51	RDSYSST	Display the status of the entire battery buffer of a CPU (0492)	96	124	59	78	25	37
51	RDSYSST	Display the status of the 24 V supply of all racks of a CPU (0592)	96	124	59	78	25	37
51	RDSYSST	Central Display the diagnostic status of the expansion devices (0692)	177	206	111	131	46	58
51	RDSYSST	Distributed Display the diagnostic status of the DP system 1 stations (via integrated DP interface) (0692)	458	505	287	318	118	132

SFC-No.	SFC-Name	Function	Execution Time in µs					
			CPU 412-3H solo	CPU 412-3H redun-dant	CPU 414-4H solo	CPU 414-4H redun-dant	CPU 417-4H solo	CPU 417-4H redun-dant
51	RDSYSST	Diagnostic status of the stations of a DP master system connected via an external DP interface (4692) First call	164	236	104	152	43	68
		Intermediate call	98	98	61	61	25	25
		Last call	108	108	66	66	28	28
51	RDSYSST	“Advanced DP master system information” partial list Display advanced information via a DP master system (0195)	102	102	64	64	27	27
		Display header information (0F95)	75	75	46	46	20	20
51	RDSYSST	“Diagnostic buffer” partial list Display all deliverable event information in the current operating mode (max. 21) (00A0)	93 - 200	93 - 200	60 - 126	60 - 126	29 - 53	29 - 53
		Display the latest entries (n = 1-23) (01A0)	93 + n* 5,1	93 + n* 5,1	58 + n* 3,5	58 + n* 3,5	24 + n* 3	24 + n* 3
		Display the header information (0FA0)	83	83	51	51	22	22

SFC-No.	SFC-Name	Function	Execution Time in µs					
			CPU 412-3H solo	CPU 412-3H redun-dant	CPU 414-4H solo	CPU 414-4H redun-dant	CPU 417-4H solo	CPU 417-4H redun-dant
51	RDSYSST	"Diagnostic data DS 0" partial list Display via logical basic address (00B1) Central	232	301	153	197	76	99
51	RDSYSST	Distributed (00B1) first call	200	242	126	153	54	68
51	RDSYSST	Distributed (00B1) intermediate call, REQ = 0	118	118	75	75	31	31
		Distributed (00B1) last call	130	130	82	82	34	34
51	RDSYSST	"Diagnostic data DR 1" partial list Display via physical address (00B2) Display a 16–byte long DR 1	166	196	109	124	69	94

SFC-No.	SFC-Name	Function	Execution Time in µs					
			CPU 412-3H solo	CPU 412-3H redun-dant	CPU 414-4H solo	CPU 414-4H redun-dant	CPU 417-4H solo	CPU 417-4H redun-dant
51	RDSYSST	“Diagnostic data DR 1” partial list Display via logical basic address (00B3) Display a 16–byte long DR 1 central	261	318	195	235	133	157
		distributed first call (00B3)	203	243	127	152	54	68
51	RDSYSST	distributed intermediate call (00B3)	118	118	75	75	31	31
		distributed last call (00B3)	140	140	89	89	37	37

DR = Data record

SFC No.	SFC Name	Function	Execution Time in µs					
			CPU 412-3H solo	CPU 412-3H redun-dant	CPU 414-4H solo	CPU 414-4H redun-dant	CPU 417-4H solo	CPU 417-4H redun-dant
51	RDSYSST	”Diagnostic Data DP Slave” partial list Display via configured diagnostic address (00B4) First call	202	240	127	151	53	68
		Intermediate call, REQ = 0 (00B4)	117	117	74	74	30	30
		Last call (6 - 240 bytes) (00B4)	138	159	109	129	36	45
52	WR_USMSG	Write user entry in diagnostic buffer write with message	75	102	67	78	18	31
		without message	58	91	41	71	18	31
54	RD_DPARAM	Read dynamic parameters local AI 8*13 bits	90	128	56	81	22	34
54	RD_DPARM	distributed AI 8*12 bits (DS1 = 14 bytes)	105	106	69	71	25	28
55	WR_PARM	Write dynamic parameters local AI 8*13 bits	250	325	171	219	92	144
		distributed First call AI 8*12 bits (14 - 240 bytes)	193	244	122	162	51	69
		distributed Intermediate/last call, REQ = 0	93	93	59	59	24	24

SFC No.	SFC Name	Function	Execution Time in µs					
			CPU 412-3H solo	CPU 412-3H redun-dant	CPU 414-4H solo	CPU 414-4H redun-dant	CPU 417-4H solo	CPU 417-4H redun-dant
56	WR_DPARM	Write predefined dynamic parameters AI 8*13 bits local	288	362	210	257	128	150
		distributed First call AI 8*12 bits (2 - 240 bytes)	157	207	100	132	41	61
		Intermediate/last call	82	82	51	51	21	21
57	PARM_MOD	Assign module parameters local Module/DS number/DS lengths in bytes AI 8*13 bits	489	607	357	430	222	256
		distributed AO 8*12 bits First call (16 - 240 bytes)	156	208	99	139	42	60
		distributed Intermediate/last call	79	79	50	50	20	21

SFC No.	SFC Name	Function	Execution Time in µs					
			CPU 412-3H solo	CPU 412-3H redun-dant	CPU 414-4H solo	CPU 414-4H redun-dant	CPU 417-4H solo	CPU 417-4H redun-dant
58	WR_REC	Write parameter data record local (n = number of bytes)	180 + n * 2,6	237 + n * 2,6	121 + n * 2,4	165 + n * 2,4	71 + n * 2,2	120 + n * 2,2
		First call, integrated DP interface module (n = number of bytes)	177 + n * 0,06	225 + n * 0,06	112 + n * 0,06	152 + n * 0,06	47 + n * 0,04	65 + n * 0,04
		Intermediate call, REQ = 0 integrated DP interface module	76	76	48	48	20	20
		Last call, integrated DP interface module	76	76	49	49	20	21
		First call, external DP interface module (n = number of bytes)	183 + n * 0,06	191 + n * 0,06	108 + n * 0,06	110 + n * 0,06	44 + n * 0,03	48 + n * 0,03
		Intermediate call, REQ = 0 external DP interface module	73	73	47	50	21	21
		Last call, external DP interface module	74	74	48	51	21	21

SFC No.	SFC Name	Function	Execution Time in µs					
			CPU 412-3H solo	CPU 412-3H redun-dant	CPU 414-4H solo	CPU 414-4H redun-dant	CPU 417-4H solo	CPU 417-4H redun-dant
59	RD_REC	Read data record local (n = number of bytes)	218 + n * 2,8	275 + n * 2,8	125 + n * 2,4	163 + n *2,4	71 + n * 2,3	96 + n * 2,4
		First call, integrated DP interface module	163	214	103	137	44	63
		Intermediate call, REQ = 0 integrated DP interface module	75	75	47	47	19	20
		Last call, integrated DP interface module (n = number of bytes)	128 + n * 0,7	128 + n * 0,7	82 + n * 0,13	83 + n * 0,13	36 + n * 0,13	37 + n * 0,13
		First call, external DP interface module	209	209	110	110	42	42
		Intermediate call, REQ = 0 external DP interface module	76	76	47	47	20	20
		Last call, external DP interface module (n = number of bytes)	119 + n * 0,1	119 + n * 0,1	92 + n * 0,07	92 + n * 0,07	37 + n * 0,02	37 + n * 0,02
62	CONTROL	Check status of the connection belonging to a local communication-SFB-instance	78	124	50	77	20	34
64	TIME_TCK	Display millisecond timer	13	48	8	31	3	11
78	OB_RT	Determining the OB Program Runtime	35	79	21	50	9	19
79	SET [1)]	Set bit array in I/O area n = number of bits to set at 1	43 + n * 1,0	112 + n * 3,7	27 + n * 0,7	80 + n * 2,5	12 + n * 0,4	34 + n * 1,3

SFC No.	SFC Name	Function	Execution Time in µs					
			CPU 412-3H solo	CPU 412-3H redun-dant	CPU 414-4H solo	CPU 414-4H redun-dant	CPU 417-4H solo	CPU 417-4H redun-dant
80	RSET [1]	Delete bit array in I/O area n = number of bits to set at 0	40 + n * 1,0	110 + n * 3,8	26 + n * 0,7	70 + n * 2,5	11 + n * 0,4	34 + n * 1,3
81	UBLKMOV	Copy variable without interruption n = number of bytes to copy	28 + n* 0,04	28 + n* 0,05	18 + n* 0,03	18 + n* 0,03	7 + n* 0,02	7 + n* 0,02
87	C_DIAG	Determine current connection status MODE = 0	22	69	14	46	6	21
		Mode = 1, 2, 3	177	558	163	356	72	320
90	H_CTRL	Influence processes involving fault-tolerant systems	13	13	8	8	3	4

[1] Measured with I/O modules of the type “Binary Simulator C79459-A1002-A1, Release 1” in the central rack

SFC No.	SFC Name	Function	Execution Time in µs					
			CPU 412-3H solo	CPU 412-3H redun-dant	CPU 414-4H solo	CPU 414-4H redun-dant	CPU 417-4H solo	CPU 417-4H redun-dant
100	SET_CLKS	Set time-of-day and clock status MODE = 1	288	613	183	565	76	248
		MODE = 2	166	502	106	327	44	159
		MODE = 3	291	617	183	577	77	251
103	DP_TOPOL	Detemine bus topology in a DP master system first call, REQ = 1	160	320	103	203	45	91
		Intermediate call	30	30	19	19	8	8
		Last call BUSY = 0	32	32	21	21	8	9
104	CIR	Controls the CiR procedure MODE = 0, information	16	–	9	–	5	–
		MODE = 1, Enable CiR procedure	16	–	9	–	5	–
		MODE = 2, Disable CiR procefure entirely	16	–	9	–	5	–
		MODE = 3, Disable CiR procedure partially	16	–	9	–	5	–

SFC No.	SFC Name	Function	Execution Time in µs					
			CPU 412-3H solo	CPU 412-3H redun-dant	CPU 414-4H solo	CPU 414-4H redun-dant	CPU 417-4H solo	CPU 417-4H redun-dant
105	READ_SI	Read dynamically assigned system resources MODE = 0	81 - 969 0)	88 - 1001 0)	51 - 592 0)	55 - 612 0)	21 - 497 0)	23 - 523 0)
		MODE = 1	107 - 1148 1)	296 - 1370 1)	72 - 712 1)	197 - 855 1)	30 - 581 1)	113 - 689 1)
		MODE = 2	107 - 936 1)	296 - 1167 1)	72 - 583 1)	198 - 725 1)	30 - 468 1)	116 - 579 1)
		MODE = 3	107 - 1151 2)	296 - 1375 2)	73 - 716 2)	204 - 859 2)	30 - 581 2)	117 - 690 2)

0) Depending on the size of the SYS_INST target area and on the number of the system resources to be read

1) Depending on the number of active messages (assigned system resources)

2) Depending on the number of active messages (assigned system resources) and on the number of assigned instances with the desired CMP_ID.

SFC No.	SFC Name	Function	Execution Time in µs					
			CPU 412-3H solo	CPU 412-3H redundant	CPU 414-4H solo	CPU 414-4H redundant	CPU 417-4H solo	CPU 417-4H redundant
106	DEL_SI	Enable dynamically assigned system resources MODE = 1	138 - 2167 1)	541 - 13125 1)	91 - 1332 1)	351 - 8034 1)	38 - 1067 1)	211 - 7181 1)
		MODE = 2	138 - 813 1)	532 - 1214 1)	92 - 509 1)	352 - 767 1)	38 - 378 1)	210 - 548 1)
		MODE = 3	137 - 2165 2)	531 - 13211 2)	91 - 1333 2)	351 - 7972 2)	38 - 1067 2)	211 - 7171 2)
107	ALARM_DQ	Acknowledgeable block-related messages create first call, SIG = 0 -> 1	262-593 1)	596-937 1)	164-385 1)	375-573 1)	67-240 1)	162-334 1)
		Call (without message)	76-397 1)	172-492 1)	45-249 1)	93-308 1)	18-182 1)	45-213 1)

1) Depending on the number of active messages (assigned system resources)

2) Depending on the number of active messages (assigned system resources) and on the number of assigned instances with the desired CMP_ID.

SFC No.	SFC Name	Function	Execution Time in µs					
			CPU 412-3H solo	CPU 412-3H redun-dant	CPUs 414-4H solo	CPU 414-4H redun-dant	CPU 417-4H solo	CPU 417-4H redun-dant
108	ALARM_D	Not acknowledgeable block-related messages create first call, SIG = 0 -> 1	260-599 2)	598-945 2)	160-374 2)	372-574 2)	71-240 2)	158-324 2)
		Call (without message)	75-399 2)	166-477 2)	45-247 2)	107-304 2)	17-183 2)	45-209 2)
109	PROTECT	Activating write protection	11	11	7	7	2	2

2) Depending on the number of active messages (assigned system resources)

System Function Blocks

The following table lists the system function blocks provided with the operating system of the S7-400 CPUs as well as the execution times of the individual CPUs (X: function exists, execution times were not available when manual was printed).

SFC No.	SFC Name	Function	Execution Time in µs					
			CPU 412-3H solo	CPU 412-3H redun-dant	CPU 414-4H solo	CPU 414-4H redun-dant	CPU 417-4H solo	CPU 417-4H redun-dant
0	CTU	Count up	4	4	2	2	1	1
1	CTD	Count down	3	4	2	3	1	1
2	CTUD	Count up and down	4	4	2	2	1	1
3	TP	Generate pulse	18	53	9	33	4	14
4	TON	Generate on-delay	15	52	9	33	4	14
5	TOF	Generate off-delay	11	11	6	7	3	3
8	USEND	Send data without coordination (one send parameter supplied) JOB activated (1 - 440 bytes)	271 - 307	398 - 462	170 - 196	267 - 289	70 - 81	114 - 124
		JOB checked	95	142	60	91	24	41
		JOB finished (DONE = 1)	91	150	58	94	24	41

SFC No.	SFC Name	Function	Execution Time in µs					
			CPU 412-3H solo	CPU 412-3H redun-dant	CPU 414-4H solo	CPU 414-4H redun-dant	CPU 417-4H solo	CPU 417-4H redun-dant
9	URCV	Receive data without coordination (one receive parameter supplied) JOB activated	79	141	51	90	21	39
		JOB checked	85	132	54	85	22	39
		JOB finished (NDR = 1; 1 - 440 bytes)	173 - 211	233 - 260	109 - 133	147 - 171	44 - 56	62 - 73
12	BSEND	Send data block by block JOB activated (1 - 3000 bytes)	233	335	146	209	60	93
		JOB checked	103	148	65	95	26	43
		JOB finished (DONE = 1)	98	157	62	100	26	43
13	BRCV	Receive data block by block JOB activated (1 - 3000 bytes)	112	182	70	110	30	46
		JOB checked	115	161	73	102	30	46
		JOB finished	100	153	61	98	25	42

SFC No.	SFC Name	Function	Execution Time in µs					
			CPU 412-3H solo	CPU 412-3H redun-dant	CPU 414-4H solo	CPU 414-4H redun-dant	CPU 417-4H solo	CPU 417-4H redun-dant
14	GET	Read data from remote CPU (one area specified) JOB activated	204	300	127	200	53	84
		JOB checked	96	142	60	90	24	41
		JOB finished (NDR = 1; 1 - 450 bytes)	173 - 216	233 - 267	108 - 138	146 - 174	45 - 56	62 - 74
15	PUT	Write data to remote CPU JOB activated (1 - 404 bytes)	285 - 319	437 - 475	178 - 203	273 - 297	74 - 84	117 - 126
		JOB checked	96	142	60	90	24	41
		JOB finished (DONE = 1)	91	149	57	95	24	41
16	PRINT	Send data to a printer JOB activated, REQ = 1	298 - 329	459 - 498	183 - 209	278 - 298	76 - 85	119 - 128
		JOB checked	102	151	58	95	24	41
		JOB finished, DONE = 1	93	148	56	92	23	41

SFC No.	SFC Name	Function	Execution Time in µs					
			CPU 412-3H solo	CPU 412-3H redun-dant	CPU 414-4H solo	CPU 414-4H redun-dant	CPU 417-4H solo	CPU 417-4H redun-dant
19	START	Start remote device JOB activated, REQ = 1	271	381	171	230	70	98
		JOB checked	101	147	63	93	26	42
		JOB finished, DONE = 1	98	156	61	99	25	42
20	STOP	Stop remote device JOB activated, REQ = 1	267	365	167	230	70	102
		JOB checked	100	147	62	92	26	42
		JOB finished, DONE = 1	97	156	60	98	25	42
21	RESUME	Restart remote device JOB activated, REQ = 1	279	387	170	230	70	98
		JOB checked	100	146	63	92	26	43
		JOB finished, DONE = 1	97	145	61	98	25	42
22	STATUS	Query status of remote partner JOB activated, REQ = 1	171	273	102	164	42	75
		JOB checked	96	142	60	89	24	41
		JOB finished, NDR = 1	263	324	165	204	68	85

SFC No.	SFC Name	Function	Execution Time in µs					
			CPU 412-3H solo	CPU 412-3H redun-dant	CPU 414-4H solo	CPU 414-4H redun-dant	CPU 417-4H solo	CPU 417-4H redun-dant
23	USTATUS	Receive status of remote device without coordination JOB activated, NDR = 1	84	144	53	90	22	39
		JOB checked	85	132	53	90	22	39
		JOB finished	264	323	165	203	68	85
31	NOTIFY_8P	Generate block–related message without acknowledgment First call or JOB activated, SIG = 0–> 1 (1 - 420 bytes)	336 - 373	505 - 541	211 - 237	343 - 368	87 - 99	143 - 158
		JOB checked	125	166	80	118	33	50
		JOB finished, DONE = 1	130	168	81	119	33	51
32	DRUM	Implement sequencer	21	71	13	44	5	22
33	ALARM	Generate block-related message with acknowledgment First call or JOB activated, SIG = 0–> 1 (1 - 420 bytes)	332 - 369	503 - 537	211 - 235	339 - 366	88 - 98	147 - 158
		JOB checked	126	172	81	112	33	50
		JOB finished, DONE = 1	131	172	81	118	33	50

SFC No.	SFC Name	Function	Execution Time in µs					
			CPU 412-3H solo	CPU 412-3H redun-dant	CPU 414-4H solo	CPU 414-4H redun-dant	CPU 417-4H solo	CPU 417-4H redun-dant
34	ALARM_8	Generate block-related message without accompanying values for 8 signals First call or JOB activated, SIG = 0–> 1 (1 - 420 bytes)	259	381	161	257	67	110
		JOB checked	124	163	81	111	33	50
		JOB finished, DONE = 1	128	169	80	118	33	51
35	ALARM_8P	Generate block-related message with accompanying values for 8 signals First call or JOB activated, SIG = 0–> 1 (1 - 420 bytes)	337 - 369	489 - 527	209 - 235	332 - 366	87 - 98	147 - 159
		JOB checked	127	163	81	110	33	50
		JOB finished, DONE = 1	129	163	80	118	33	50
36	NOTIFY	Generate block-related message without acknowledgment First call or JOB activated, SIG = 0–> 1 (1 - 420 bytes)	331 - 367	502 - 538	207 - 233	338 - 356	86 - 97	146 - 154
		JOB checked	123	173	80	109	33	50
		JOB finished, DONE = 1	129	177	80	119	33	54

SFC No.	SFC Name	Function	Execution Time in µs					
			CPU 412-3H solo	CPU 412-3H redun-dant	CPU 414-4H solo	CPU 414-4H redun-dant	CPU 417-4H solo	CPU 417-4H redun-dant
37	AR_SEND	Send archive data First call or JOB activated, REQ = 1 (1 - 3000 bytes)	243	324	146	219	60	88
		JOB checked	109	149	65	96	27	44
		JOB finished, DONE = 1	109	149	63	102	26	44
52	RDREC	Read data record from a DP slave via integrated DP interface, First call (2-16 bytes)	173	224	110	150	46	65
		Intermediate call	84	84	53	53	21	21
52	RDREC	Last call	140	140	90	90	42	42
52	RDREC	Read data record from a DP slave via external DP interface, First call (4-16 bytes)	173	224	109	150	43	64
52	RDREC	Intermediate call	84	84	53	53	21	21
52	RDREC	Last call	141	141	90	90	38	38

SFC No.	SFC Name	Function	Execution Time in µs					
			CPU 412-3H solo	CPU 412-3H redun-dant	CPU 414-4H solo	CPU 414-4H redun-dant	CPU 417-4H solo	CPU 417-4H redun-dant
53	WRREC	Write data record in a DP slalve via integrated DP interface, First call (1-10 bytes)	185	236	116	158	49	67
		Intermediate call	82	82	53	53	21	21
		Last call	84	84	53	53	22	22
53	WRREC	Write data record in a DP slave via external DP interface, First call (2-14 bytes)	184	236	117	158	45	47
53	WRREC	Intermediate call	82	82	53	53	21	21
		Last call	84	84	53	53	22	22
54	RALRM	Receive interrupt from a DP slave Runtime measurement for non-I/O-dependent OBs, MODE = 1, OB 1	83	83	49	49	21	21
54	RALRM	Receive interrupt from a DP slave Runtime measurement at integrated DP interface, MODE = 1, OB 40, OB 83, OB 86	254	254	135	135	65	65
		OB 55 to OB 57, OB 82	263	263	141	141	67	67
		OB 70	254	254	133	133	61	61

SFC No.	SFC Name	Function	Execution Time in µs					
			CPU 412-3H solo	CPU 412-3H redun-dant	CPU 414-4H solo	CPU 414-4H redun-dant	CPU 417-4H solo	CPU 417-4H redun-dant
54	RALRM	Receive interrupt from a DP slave Runtime measurement at external DP interface, MODE = 1, OB 40, OB 83, OB 86	397	397	231	231	105	105
		OB 55 to OB 57, OB 82	713	713	412	412	191	191
		OB 70	457	457	233	233	211	211
54	RALRM	Receive interrupt from a DP slave Runtime measurement at central I/O, MODE = 1, OB 40, OB 82, OB 83, OB 86	136	136	79	79	37	37
		OB 55 to OB 57	578	578	331	331	151	151

Sublist of the System Status List (SSL)

SSL-ID	Information Functions
	Module Identification
0111	One ident. data record only
	CPU Characteristics
0012	CPU features, all features
0112	Features of a group
0F12	Only SSL partial list header information
	User Memory Area
0F12	Only partial list header information
	User Memory Area
0113	Data record for specified memory area
	Work memory
	System Areas
0014	System areas, all system areas
0F14	Only partial list header information
	Block Types
0015	Block types, data records for all block types

	Status Module LEDs
0019	Status of all module LEDs
0F19	Only partial list header information
	Component Identification
001C	Identification of all components
011C	Identification of one component
021C	Identification of all components of an H–system CPU
031C	Identification of a component of all redundant CPUs of an H-system
0F1C	Only SSL partial list header information
	Interrupt Status
0222	Data record for specified interrupt
	Assignment between process image partitions and OBs
0025	Assignment betweeen all process image partitions and OBs within the CPU
0125	Assignment between a process image partition and the corresponding OB
0225	Assignment between an OB and the corresponding process image partitions
0F25	Only SSL partial list header information

Sublist of the System Status List (SSL), continued

	Communication Status Data
0132	Status data for a communication unit
0232	Status data for a communication unit
	H CPU Group Information
0071	Information on the current status of the H system
0F71	Only partial list header information
	Status of the Module LEDs
0174	Status of one LED
	Switched DP Slaves in the H System
0C75	Communication status between the H system and a switched DP slave
	DP Master System Information
0090	Information about all the DP master systems known to the CPU
0190	Information about a DP master system
0F90	Only SSL partial list header information

Sublist of the System Status List (SSL), continued

	Module Status Information (A maximum of 27 data records are supplied)
0591	Module status information of all submodules of the host module
0991	Status information of all submodules in the host module in the rack
0C91	Status information of a module in the central rack or connected to an integrated DP interface module via the logical base address
4C91	Status information of a module connected to an external DP interface module via the logical base address
0D91	Status information of all modules in the specified rack

Sublist of the System Status List (SSL), continued

SSL-ID	Information Functions
	Rack/Station Status Information
0092	Expected status of the central racks/stations of a DP master system
4092	Expected status of the stations of a DP master system which is connected via an external DP interface module
0292	Actual status of the central racks/stations of a DP master system
4292	Actual status of the stations of a DP master system which is connected via an external DP interface module
0392	Status of the back–up battery of a CPU rack if at least one battery fails
0492	Status of the entire back–up batteries of all racks of the a CPU
0592	Actual status of the racks in the central configuration/stations of DP master system which is connected via an external DP interface module.
0692	OK status of the expansion units in the central configuration/stations of a DP master system which is connected via an integrated DP interface module.
4692	OK status of the stations of a DP master system which is connected via an external DP interface module.

SSL-ID	Information Functions
	Addtional DP Master System Information
0195	Additional information on a DP master system
0F95	Only partial list header information
00A0	All current diagnostic entries available in current operating mode
01A0	Last x entries. X is listed in index
0FA0	Only partial list header information
	Module Diagnostic Data
00B1	First four diagnostic bytes of a module (DS0)
00B2	All diagnostic data of a module (≤ 220 bytes, DS1) (no DP module)
00B3	All diagnostic data of a module (≤ 220 bytes, DS1)
00B4	Diagnostic data of a DP slave with logical base address

Alphabetical Index of Instructions