IQR-1C-QY000698

Dec. 6. 2005

RELIABILITY DATA

DEVICE TYPE: UPD97281GF-202-3BA-A

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Table.1 Reliability Test Item

Item	Symbol	Test Condition		Pass/Fail criteria
High Temp. with bias	BT	Ta＝125℃	VDD＝3.6 V	According to electrical characteristics standard
High Temp. Storage	HT	Ta＝150℃		
Temp. Cycling	T／C	Pre-Treatment (See Table.2)	-65℃ ～ 150℃ (30min) (30min)	
Pressure Cooker	PCT		Ta=125℃,RH=100%,2.3atm	
High Humid. with bias	HHBT		Ta=85℃, RH=85%, VDD＝3.6 V	

Table. 2 Pre-Treatment for T/C, PCT, HHBT

Symbol	Pre-Treatment Condition							
T/C HHBT PCT	Temp. Cycling (20cyc.)	→	Bake 125℃ 20hrs.	→	Humid. Storage 30℃/70%RH 178hrs.	→	Infrared Reflow 3 times (260℃ Peak)	

Table. 3 Reliability Test Result

(*) ･･･See Table.1,2

Device	Package		Test (*)	n	Test Results				Remarks
	Type	Pin	Item						
D97281GD	QFP	100	BT	24	Hour	168	1000		
					NG	0	0		
			HT	20	Hour	168	1000		
					NG	0	0		
			HHBT	24	Hour	168	1000		
					NG	0	0		
			T/C	25	Cycle	100	300		
					NG	0	0		
			PCT	20	Hour	96	192		
					NG	0	0		

ESD DATA

1. TEST CONDITION (A)

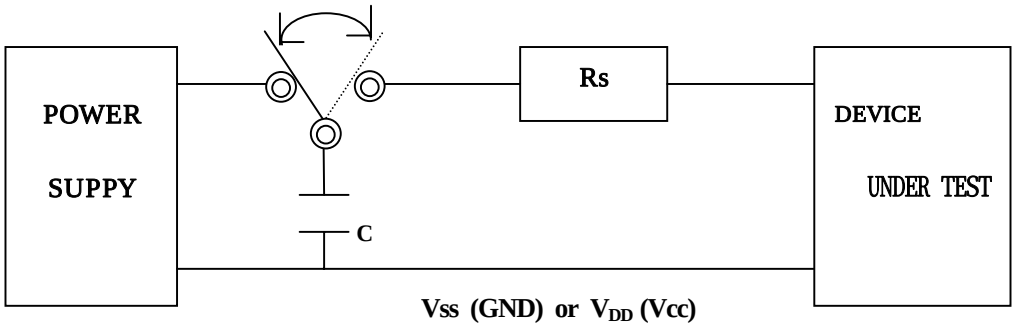
(1) C= 200pF, Rs=0Ω

(2) 5 TIMES FORCE TO EACH PINS AGAINST V_{SS} (GND) OR V_{DD} (V_{CC}).

2. TEST RESULT

CONDITION	FORCING VOLTAGE & POLARITY	GND CONDITION	FORCING TIMES	SAMPLE SIZE	# OF FAILURE
I	+200V VOLTAGE FORCE TO EACH PINS	Vss (GND)=0V	5 TIMES	5 PCS	0
II	-200V VOLTAGE FORCE TO EACH PINS	Vss (GND)=0V	5 TIMES	5 PCS	0
III	+200V VOLTAGE FORCE TO EACH PINS	V_{DD} (Vcc)=0V	5 TIMES	5 PCS	0
IV	-200V VOLTAGE FORCE TO EACH PINS	V_{DD} (Vcc)=0V	5 TIMES	5 PCS	0

3. TEST CIRCUIT



ESD DATA

1. TEST CONDITION (B)

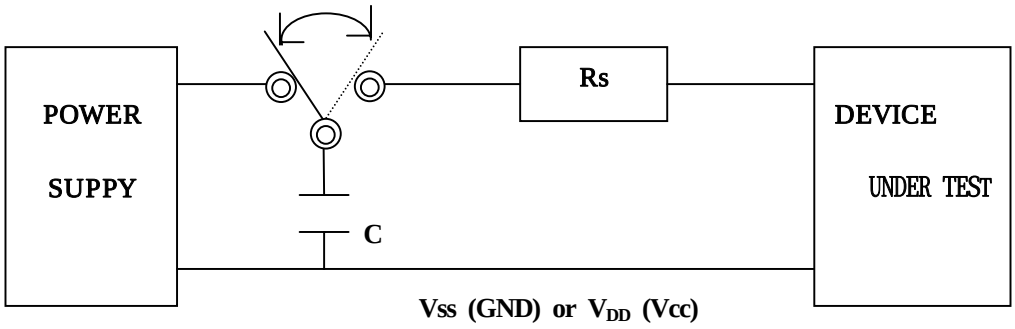
(1) C= 100pF, Rs=1.5KΩ

(2) 5 TIMES FORCE TO EACH PINS AGAINST V_{SS} (GND) OR V_{DD} (V_{CC}).

2. TEST RESULT

CONDITION	FORCING VOLTAGE & POLARITY	GND CONDITION	FORCING TIMES	SAMPLE SIZE	# OF FAILURE
I	+2000V VOLTAGE FORCE TO EACH PINS	Vss (GND)=0V	5 TIMES	5 PCS	0
II	-2000V VOLTAGE FORCE TO EACH PINS	Vss (GND)=0V	5 TIMES	5 PCS	0
III	+2000V VOLTAGE FORCE TO EACH PINS	V_{DD} (Vcc)=0V	5 TIMES	5 PCS	0
IV	-2000V VOLTAGE FORCE TO EACH PINS	V_{DD} (Vcc)=0V	5 TIMES	5 PCS	0

3.TEST CIRCUIT



LATCH-UP DATA

Ta=25°C

(N=5, V_{DD}=3.6V)

	TEST METHOD (TEST CIRCUIT)	LATCH-UP THRESHOLD CURRENT / VOLTAGE
I	DC CURRENT INJECTION (Fig, 1-a,b)	$\lvert I_2 \rvert$ > 500mA

LATCH-UP TEST PROCEDURE

- DC CURRENT INJECTION -

1). Set the test circuit as shown in Fig. 1-a for positive current injection, Fig. 1-b for Negative current injection.

2). Set V1 to V_{DD} max, and V2 to 0V.

3). Set all untested inputs to V_{DD} or GND.

4). Set all untested outputs to open.

5). Measure I1 and set the current limit of V1 to 2 × I1 or about appropriate value.

6). Apply V2 and increase until I1 reaches current limit (Latch up) or until V2 reaches 2 × V1.

7). Measure the value of I2 when Latch up observed.
→ Latch up threshold current

8). Remove V1&V2 supply immediately after I2 measure.

9). Repeat from 2). To 8) for all inputs and outputs.

Fig. 1-a Positive Current Injection Circuit

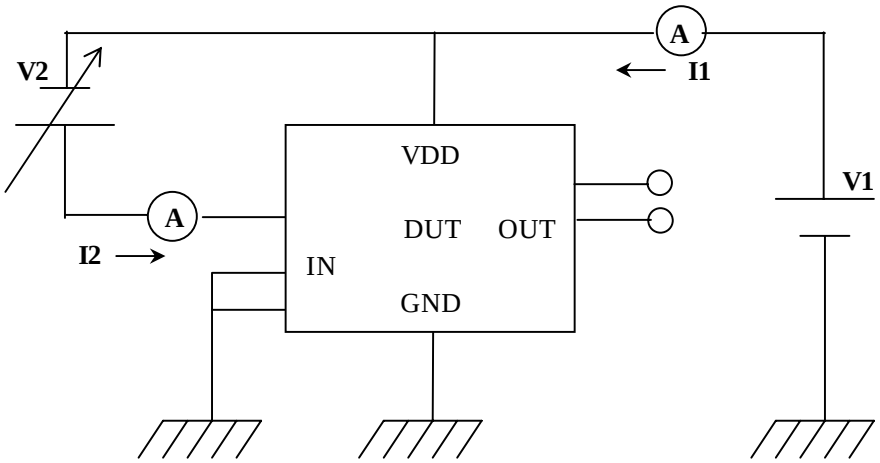


Fig. 1-b Negative Current Injection Circuit