Customer Information	V1.2

Title

Delta DPC31 Step B/DPC31 Step C1

The purpose of the following brief description is to facilitate for the user the transition from DPC31 Step B to DPC31 Step C1. For this reason, the major differences are described on the following pages. It is also recommended to download the complete documentation from the Internet. (http://www.siemens.com/comdec → PROFIBUS Descriptions, free of charge).

Contents

1 Power Consumption

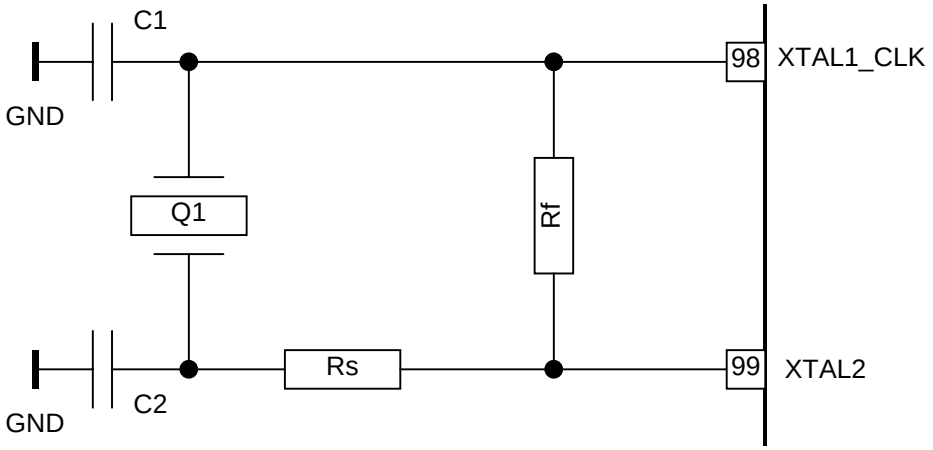
1.1 DPC31 Step B

Power Loss:	(all values typically measured)
Asynchronous:	Approx. 200mW at 12 MBd
Synchronous:	Approx. 3 mW at 31.25 kBd and 2MHz clock pulse (C31 switched off) Approx. 3 mW at 31.25 kBd and 2MHz clock pulse (C31 core @ 1MHz) Approx. 5 mW at 31.25 kBd and 4MHz clock pulse (C31 core @ 2MHz) Approx. 20 mW at 31.25 kBd and 8MHz clock pulse (C31 core @ 4MHz) Approx. 43 mW at 31.25 kBd and 16MHz clock pulse (C31 core @ 8MHz)

1.2 DPC31 Step C1

Power Loss:	(all values typically measured)
Asynchronous:	Approx. 150 mW at 12 MBd
Synchronous:	Approx. 2 mW at 31.25 kBd and 2MHz clock pulse (C31 switched off) Approx. 2 mW at 31.25 kBd and 2MHz clock pulse (C31 core @ 1MHz) Approx. 4 mW at 31.25 kBd and 4MHz clock pulse (C31 core @ 2MHz) Approx. 15 mW at 31.25 kBd and 8MHz clock pulse (C31 core @ 4MHz) Approx. 33 mW at 31.25 kBd and 16MHz clock pulse (C31 core @ 8MHz)

2 Oscillator Wiring



Hardware Versions		DPC31 Step C1	DPC31 Step B	Unit
Component	**Name**	**Value**	**Value**	
Quartz (Epson Type: MA505, MA506, MA406, MA406H)	Q1	12	12	MHz
Serial resistance	Rs	2.7	---	kΩ
Parallel resistance	Rf	1.0	---	MΩ
	C1	22	35	pF
	C2	22	35	pF

Table 2-1: Component Values for Oscillator Wiring

3 Electrical Specification

3.1 Maximum Limits

Hardware Versions		DPC31 Step C1		DPC31 Step B		Unit
Parameter	**Name**	**Condition**	**Limits**	**Condition**	**Limits**	
DC power supply	V_{DD}		-0.3 to +4.0		-0.5 to +4.6	V
Input voltage[1]	V_I		-0.3 to +6.0		-0.5 to +6.6 and $V_I < V_{DD} + 3.0$	V
Output voltage[2]	V_O		-0.3 to +6.0[3]		-0.5 to +6.6 and $V_o < V_{DD} + 3.0$	V
DC output current	I_O	I_{OL} = 4.0mA	-13	I_{OL} = 3.0mA	10	mA
	I_O	I_{OL} = 8.0mA	-26	I_{OL} = 9.0mA	30	mA
Ambient temperature	T_{opt}		-40 to +85		-40 to +85	°C
Storage temperature	T_{stg}		-55 to +125		-65 to +150	°C
Power loss for PQFP-100	P_{vmax}		800		530	mW
Junction temperature	ϑ_{jmax}		125		125	°C
R_{th} junction case	$R_{thj\rightarrow c}$		---[4]		10 (measuring point middle of casing)	K/W
R_{th} case-ambient	$R_{thc\rightarrow a}$		---[16]		85	K/W
R_{th} junction ambient	$R_{thj\rightarrow a}$		27,8		---	K/W

Table 3-1: Maximum Limits

3.2 Permitted Operating Values

Hardware Versions		DPC31 Step C1		DPC31 Step B (NEC)		Unit
Parameter	**Name**	**Min.**	**Max.**	**Min.**	**Max.**	
DC power supply	V_{DD}	3.0	3.6	3.0	3.6	V
Input voltage (low level)[5]	V_{IL}	0	0.8	0	0.8	V
Input voltage (high level)	V_{IH}	2.0	5.5	2.0	5.5	V
Input voltage (low level)[6]	V_{IL}	0	0.7	0	0.8	V
Input voltage (high level)	V_{IH}	2.1	5.5	2.0	5.5	V
Input rise time	t_r	0	200	0	200	ns
Input decay time	tf	0	200	0	200	ns
Busfigh time	t_{BF}	0	20	0	20	ns
Schmitt trig. Input rise time	t_r	0	10	0	10	ms
Schmitt trig. Input decay time	tf	0	10	0	10	ms

Forr Ta = -40 ... +85 °C

Table 3-2: Permitted Operating Values

[1] The exception pin 98 is not listed separately here, as it is not listed separately in Step B either.
[2] The exception pins 95, 96, and 99 is not listed separately here, as they are not listed separately in Step B either.
[3] The output itself can supply a maximum voltage of Vdd+0.3V. Greater voltages at the output pins have an external cause, e.g. pullup resistances
[4] These values are no longer specified by Amkor (casing manufacturer)
[5] With Step C1, does not apply to input pins 6, 87, 88, and 98
[6] With Step C1, does not apply to input pins 6, 87, and 88

3.3 Power Up of Supply Voltage

If the DPC31 Step C1 is used in modules with a mixed power supply (3.3V and 5V), the following is to be noted:
All pins except Pin 95, 96, 98 and 99:

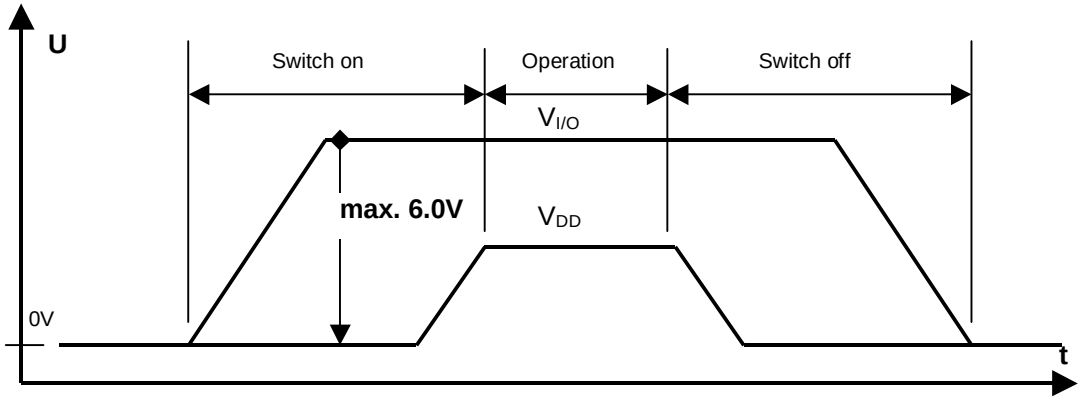


Figure 3.3-1: Voltage Ramp for 5V Tolerant I/Os

During the switching on/off process, the voltage on the 5V tolerant signal pins is not to exceed a value of +6.0V and is not to drop below a value of –0.3V.
The 5V tolerant outputs can drive only a voltage of –0.3V to VDD+0.3V. A higher voltage at the pin can be caused only by external components; such as pullup resistors.

Exceeding these values is impermissible and can cause the DPC31 to be destroyed.

Only Pins 95, 96, 98 and 99:

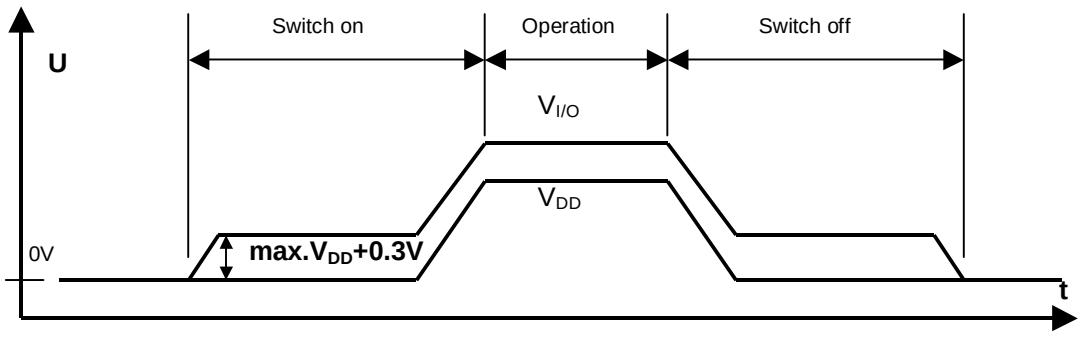


Figure 3.3-2: Voltage Ramp for LVTTL I/Os

During the switching on/off process, voltage on the specified signal pins is not to exceed a value of V_{DD}+0.3V and not drop below the value of –0.3V.

Exceeding these values is impermissible and can cause the DPC31 to be destroyed.

3.4 Structure of the Pad Cells with 5V Tolerance

3.4.1 Step B

The input pad cells used have a tolerance of 5V; that is, they are provided with a protective circuit. This means that, although they are supplied internally with only 3.3V, the input level may be 5.5V maximum. Table 3.3 shows the operating points.
The 5V-tolerant output pad cells are also provided with a special protective circuit. When driving the 0-level, there is no difference with respect to the conventional pad cells. The 1-level is driven actively up to V_{DD} - 0.3V. Starting with this voltage, the external pull-up resistor pulls the level to **V_{DD2} (5V).** This pull-up is needed only if a 5V-CMOS input is to be driven. For reasons of interference immunity, TTL-level is recommended.

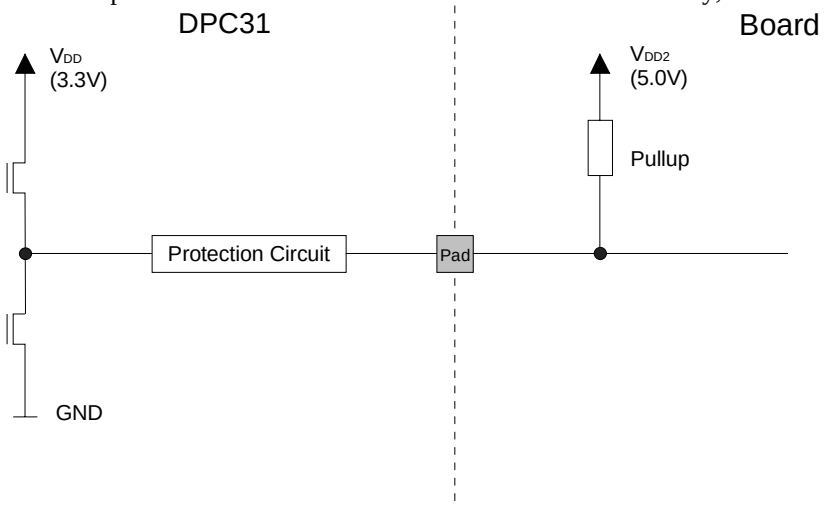


Figure 3.4-1: Wiring of an Output Pad Cell with 5V Tolerance of Step B

3.4.2 Step C1

The input pad cells used have a tolerance of 5V; that is, they are provided with a protective circuit. This means that, although they are supplied internally with only 3.3V, the input level may be 6 V maximum. Table 3.3 shows the operating points.
The 5V-tolerant output pad cells are also provided with a special protective circuit. When driving the 0-level, there is no difference with respect to the conventional pad cells. The 1-level is driven actively up to V_{DD} - 0.3V. Starting with this voltage, the external pull-up resistor pulls the level to **V_{DD} (3,3V) +0,6V**. This pull-up is needed only if a 5V-CMOS input is to be driven. For reasons of interference immunity, TTL-level is recommended.

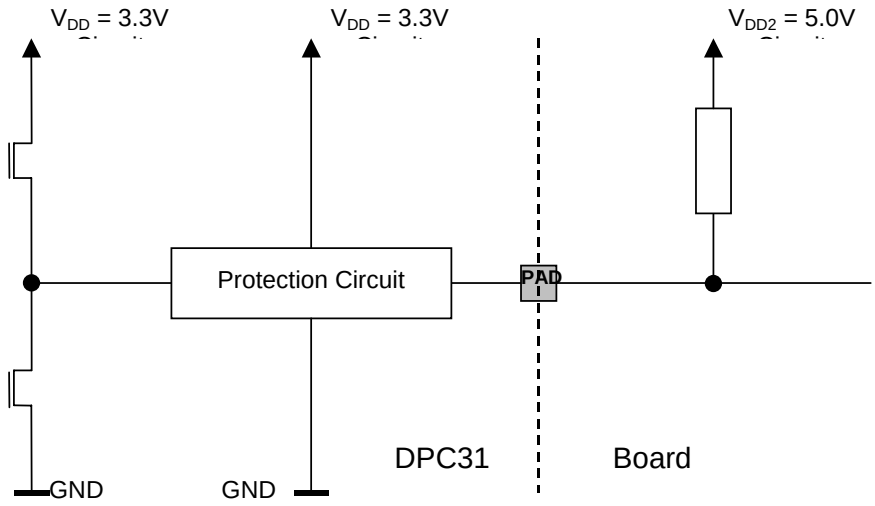


Figure 3.4-2: Wiring of an Output Pad Cell with 5V Tolerance of STEP C1

3.5 DC Specification of the Pad Cells

Hardware Versions			DPC31 Step C1			DPC31 Step B			Unit
Parameter	**Name**	**Condition**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	
Input Voltage 0 Level[7]	V_{IL}		0		0.8	0		0.8	V
Input Voltage 1 Level[7]	V_{IH}		2.0		5.5	2.0		5.5	V
Output Voltage 0 Level[8]	V_{OL}	I_{OL} = 0 mA			0.1			0.1	V
Output Voltage 1 Level[8]	V_{OH}	I_{OH} = 0 mA	V_{DD} – 0.2		V_{DD}+0.6[9]	V_{DD} – 0.2		5.5[10]	V
Output Voltage 1 Level[11]	V_{OH}	I_{OH} = 0 mA	V_{DD} – 0.2		V_{DD}	V_{DD}-0.2.			V
Schmitt Trig. +ve threshold[12]	V_P				2.1	1.2		2.4	V
Schmitt Trig. -ve threshold[12]	V_N		0.7			0.6		1.8	V
Schmitt Trig. hysteresis[12]	V_H		0.4			0.3		1.5	V
Schmitt Trig. Input Voltage[12]	V_{IH}				5.5			.	V
Input leakage current	I_I	$V_I = V_{DD}$ or GND			±1		$\pm 10^{-5}$	±10	µA
Output Current 0 Level 4 mA cell / 5V tolerant[13]	I_{OL}	V_{OL} = 0.4 V V_{DD} = 3V T_J = 95°C	3.84			3			mA
Output Current 1-Level 4 mA cell / 5V tolerant[23]	I_{OH}	V_{OH} = 2.4 V V_{DD} = 3V T_J = 95°C	–3.84			–2			mA
Output Current 0 Level 8 mA cell / 5V tolerant[14]	I_{OL}	V_{OL} = 0.4 V V_{DD} = 3V T_J = 100°C	7.68			9			mA
Output Current 1-Level 8 mA cell / 5V tolerant[24]	I_{OH}	V_{OH} = 2.4 V V_{DD}= 3V T_J = 95°C	–7.68			–2			mA
Output Current 0 Level 8 mA cell / 3.3V[24]	I_{OL}	V_{OL} = 0.4 V V_{DD} = 3V T_J = 95°C	7.68			9			mA
Output Current 1 Level 8 mA cell / 3.3V[24]	I_{OH}	V_{OH} = 2.4 V V_{DD} = 3V T_J = 95°C	–7.68			–9			mA
Output Current 0 Level XTAL2 pin / 3.3V[24]	I_{OH}	V_{OH} = 2.4 V V_{DD} = 3V T_J = 95°C	1.92			k.A			mA
Output Current 1 Level XTAL2 pin / 3.3V[24]	I_{OH}	V_{OH} = 2.4 V V_{DD} = 3V T_J = 95°C	–1.92			k.A.			mA
Tristate output leakage current	I_{OZ}	$V_O = V_{DD}$ or GND			±10			±10	µA
Short circuit current	I_{OS}	V_O = 0 V			–250			–250	mA
Input capacity	C_{IN}	@ f = 1 MHz		10	20		10	20	pF
Output capacity	C_{OUT}	@ f = 1 MHz		10	20		10	20	pF
I/O capacity	$C_{I/O}$	@ f = 1 MHz		10	20		10	20	pF

Table 3-3: DC Specification for Pad Cells

[7] All inputs without pins 6, 87, 88 and 98
[8] All outputs without pins 95, 96 and 99
[9] Each output can cause a maximum level of V_{DD} to flow; if a higher level exists at an ouput, this is dependent on an external component, e.g., pull-up resistors
[10] Each output can cause a maximum level of V_{DD} to flow; if a higher level exists at an ouput, this is dependent on an external component, e.g., pull-up resistors
[11] Applies to pins 95, 96, 99
[12] Applies only to pins 6, 87 and 88
[13] 4 mA cells for Step C1, 3mA cells for Step B
[14] 8 mA cells for Step C1, 9 mA cells for Step B

4 Driver Capability

The execution time at the block outputs always depends on the driver capacity of the pad cells, as well as on the assumed capacitive load. The capacitive load on which the following timing specifications are based is provided in Table 4-1: . To specify the maximum and minimum execution time, the variations of the temperature- and supply voltage range were included also.

Signal Name	Direction	Type of Driver	Voltage	Capacity Step C1	Capacity Step B	Load
PA	In/Out	Tristate	5V tolerant	4 mA	3 mA	120 pF **
PB	In/Out	Tristate	5V tolerant	4 mA	3 mA	80 pF
PC	In/Out	Tristate	5V tolerant	4 mA	3 mA	80 pF
PD	In/Out	Tristate	5V tolerant	4 mA	3 mA	80 pF
ALE	In/Out	Tristate	5V tolerant	4 mA	3 mA	80 pF
XPSEN ***	In/Out	Tristate	5V tolerant	4 mA	3 mA	10 pF
XCSDATA	Out	Tristate	5V tolerant	4 mA	3 mA	80 pF
XCSCODE	Out	Tristate	5V tolerant	4 mA	3 mA	80 pF
PE	In/Out	Tristate	5V tolerant	8 mA	9 mA	100 pF
PF	In/Out	Tristate	5V tolerant	4 mA	3 mA	100 pF
PG	In/Out	Tristate	5V tolerant	4 mA	3 mA	100 pF
PH	In/Out	Tristate	5V tolerant	4 mA	3 mA	100 pF
SSCLK	Out	Tristate	5V tolerant	8 mA	9 mA	100 pF
SSDO	Out	Tristate	5V tolerant	8 mA	9 mA	100 pF
CLKOUT1X2	Out	Tristate	5V tolerant	8 mA	9 mA	50 pF
CLKOUT1X4	Out	Tristate	5V tolerant	8 mA	9 mA	50 pF
RTS_TXE	Out	Tristate	3.3V *	8 mA	9 mA	50 pF
TXD_TXS	Out	Tristate	3.3V *	8 mA	9 mA	50 pF

*) No pullup resistors! **) Including the capacity of the emulator connection (70pF)
***) XPSEN only for activating the emulator; otherwise use XCSCODE

Table 4-1: Identification Data of the Outputs

If in reality, the capacitive load should deviate from the assumed values, there is a change of 0.7ns maximum per 10pF.

5 Timing Diagrams

5.1 Clock Outputs

If PLL (XPLLEN = '0') is switched on:

In this operating mode, the two clock outputs are derived from the output pulse of the PLL. The clock outputs thus have the inaccuracy of the PLL (Step C1: frequency stability: ±200ppm; phase jitter: 3 ns maximum; Step B frequency stability: ±400ppm; phase jitter: 1.5 ns max). The electrical parameters are provided in Table 5-1: **Clock Outputs**.

Hardware Versions Parameter	DPC31 Step C1 min	 max	DPC31 Step B min	 max	Units
Pulse Duty Factor CLKOUT1X2 (Hi:Low)			35:65	65:35	
Pulse Duty FactorCLKOUT1X4 (Hi:Low)			35:65	65:35	
BuiltUp Time(of the PLL)		1		0.2	ms
Frequency Stability (of the PLL)		±200		±400	ppm

Table 5-1: Clock Outputs

5.2 Profibus Interface

No.	Hardware Versions Parameter		DPC31 Step C1 Min	 Max	DPC31 Step B Min	 Max	Unit
1	RTS ↑ to TXD Setup Time	XAsyn/Syn = low	7T	$7T + T_{BIT}$	4 T	$4T + T_{BIT}$	ns
		XAsyn/Syn = high	0		0		ns
2	RTS ↓ to TXD Hold Time	XAsyn/Syn = low	5T		5T	6T	ns
		XAsyn/Syn = high	0		0		ns

T: Pulse period

T_{BIT}: Pulse period of the transmission pulse of the Profibus Interface

XCTS_RXA = '0' !

Table 5-2: Specification of the Profibus Interface

6 µP Interface

6.1 Synchronous Intel Mode (80C32)

Hardware Versions		DPC31 Step C1		DPC31 Step B		
No.	Parameter	Min	Max	Min	Max	Unit
1	Address to ALE ↓ Setuptime	10		10		ns
2	Address ($AB_{8..15}$) Holdtime after XRD ↑ or XWR ↑	5		5		ns
3	XRD ↓ to Data Out (access to RAM)		4T + 14		4T+27	ns
	XRD ↓ to Data Out (access to the registers)		4T + 14		4T+27	ns
4	ALE ↓ to XRD ↓	20		20		ns
5	Data Holdtime after XRD ↑	1.5	5	3	8	ns
6	Data Holdtime after XWR ↑	10		10		ns
7	Data Setuptime to XWR ↑	10		10		ns
8	XRD ↑ to ALE ↑	10		10		ns
10	XRD Pulse Width	6T - 10		6T – 10		ns
11	XWR Pulse Width	4T		4T		ns
12	Address Holdtime after ALE ↓	10		10		ns
13	ALE Pulse Width	10		10		ns
14	XRD, XWR Cycle time	6T + 30		6T + 30		ns
15	ALE ↓ to XWR ↓	20		20		ns
16	XWR ↑ to ALE ↑	10		10		ns

Table 6-1: Timing Values in the Synchronous Intel Mode

6.2 Asynchronous Intel Mode (X86 Mode)

Hardware Versions		DPC31 Step C1		DPC31 Step B		
No.	Parameter	Min	Max	Min	Max	Unit
20	Address Setuptime to RXD ↓ or XWR ↓	0		0		ns
21	XRD ↓ to Data valid (access to RAM)		4T+14		4T+27	ns
	XRD ↓ to Data valid (access to the registers)		4T+14		4T+27	ns
22	Address ($AB_{12..0}$) Holdtime after XRD or XWR ↑	0		0		ns
23	XCS ↓ Setuptime to XRD ↓ or XWR ↓	0		-5		ns
24	XRD Pulse Width	6T (in Sim!)		6T – 10		ns
25	Data Holdtime after XRD ↑	1.5	5	3	8	ns
26	Read/Write Inactive Time	10		10		ns
27	XCS Holdtime after XRD ↑ or XWR ↑	0		0		ns
28	XRD/XWR ↓ to XRDY ↓ (Normal Ready)	4T	5T+ 14		5T + 25	ns
29	XRD/XWR ↓ to XRDY ↓ (Early Ready)	3T	4T+ 14		4T + 25	ns
30	XREADY Holdtime after XRD or XWR	7	19	4	25	ns
31	Data Setuptime to XWR ↑	10		10		ns
32	Data Holdtime after XWR ↑	10		10		ns
33	XWR Pulse Width	4T		4T		ns
34	XRD, XWR Cycle time	6T		6T		ns
35	last XRD ↓ to XCS ↓	4T + 10		4T+10		ns
36	XCS ↑ to next XWR ↑	4T		4T		ns
37	XWR ↑ to next XWR ↑ (XCS don't care)	6T		6T		ns

Table 6-2: Timing Values in the Asynchronous Intel Mode

6.3 Synchronous Motorola Mode (E_Clock Mode, for example, 68HC11)

Hardware Versions		DPC31 Step C1		DPC31 Step B		
No.	Parameter	Min	Max	Min	Max	Unit
40	E_Clock Pulse Width	4T + 67		4T + 67		ns
41	Address ($AB_{12..0}$) Setuptime to E_Clock ↑	10		10		ns
42	Address ($AB_{12..0}$) Holdtime after E_Clock ↓	5		5		ns
43	E_Clock ↑ to Data Active Delay	3.5	10	3		ns
44	E_Clock ↑ to Data valid (access to RAM)		4T + 14		4T + 27	ns
	E_Clock ↑ to Data valid (access to the registers)		4T + 14		4T + 27	ns
45	Data Holdtime after E_Clock ↓	2	5.5	3	8	ns
46	R_W Setuptime to E_Clock ↑	10		10		ns
47	R_W Holdtime after E_Clock ↓	5		5		ns
48	XCS Setuptime to E_Clock ↑	0		0		ns
49	XCS Holdtime after E_Clock ↓	0		0		ns
50	Data Setuptime to E_Clock ↓	10		10		ns
51	Data Holdtime after E_Clock ↓	10		10		ns

Table 6-3: Timing Values for the Synchronous Motorola Mode

6.4 Asynchronous Motorola Mode (for example, 68HC16)

Hardware Versions		DPC31 Step C1		DPC31 Step B		
No.	Parameter	Min	Max	Min	Max	Unit
60	Address Setuptime to AS ↓	0		0		ns
61	AS ↓ to Data valid (Access to RAM)		4T + 14		4T + 27	ns
	AS ↓ to Data valid (access to the registers)		4T + 14		4T + 27	ns
62	Address ($AB_{12..0}$) Holdtime after AS ↑	10		10		ns
63	R_W ↓ Setuptime to AS ↓	10		10		ns
64	AS Pulse Width	6T - 10		6T – 10		ns
65	Data Holdtime after AS ↑	2	5	3	8	ns
66	AS Inactive Time	10		10		ns
67	R_W Holdtime after AS ↑	10		10		ns
68	XCS ↓ Setuptime to AS ↓	-5		-5		ns
69	XCS Holdtime after AS ↑	0		0		ns
70	AS ↓ to XDSACK ↓ (Normal Ready)	4T	5T + 14		5T + 25	ns
71	AS ↓ to XDSACK ↓ (Early Ready)	3T	4T + 14		4T + 25	ns
72	XDSACK-Holdtime after AS ↑ (Normal Ready)	7.5	19	4	25	ns
72	XDSACK-Holdtime after AS ↑ (Early Ready)	7.5	19	4	25	ns
73	AS Cycle time	Wr: 5T Rd: 6T		6T		ns
74	Data Setuptime to AS ↑	10		10		ns
75	Data Holdtime after AS ↑	10		10		ns
76	AS Pulse Width	4T		4T		ns
77	last AS ↓ (Read) to XCS ↓	4T + 10		4T+10		ns
78	XCS ↑ to next AS ↑ (Write)	4T		4T		ns
79	AS ↑ to next AS ↑ (Write, XCS don't care)	6T		6T		ns

Table 6-4: Timing Values for the Asynchronous Motorola Mode

6.5 C31 Memory Interface (internal C31 on external memory)

Hardware Versions		DPC31 Step C1		DPC31 Step B		
Symbol	Parameter	Min	Max	Min	Max	Unit
t_{RLRH}	XRD pulse width	12T + 1.8		12T – 0.7		ns
t_{WLWH}	XWR pulse width	12T + 1.9		12T – 0.8		ns
t_{LLAX2}	Address hold after ALE	4T - 4.3		4T + 1.9		ns
t_{RLDV}	XRD to valid data in		10T – 33.9		10T – 33.9	ns
t_{RHDX}	Data hold after XRD	0		0		ns
t_{RHDZ}	Data float after XRD		4T – 2.3		4T + 1.1	ns
t_{LLDV}	ALE low to valid data in		16T – 31.7		16T – 31.7	ns
t_{AVDV}	Address to valid data in		18T – 41.7		18T – 41.7	ns
t_{LLWL}	ALE to XWR or XRD	6T + 0.3	6T + 1.5	6T + 1.0	6T + 2.5	ns
t_{AVWL}	Address valid to XWR or XRD	8T – 9.6		8T – 7.3		ns
t_{WHLH}	XWR or XRD high to ALE high	2T – 1.8	2T – 0.3	2T – 2.0	2T – 0.8	ns
t_{QVWX}	Data valid to XWR↓	2T – 8.0		2T – 6.5		ns
t_{QVWH}	Data setup to XWR	14T – 3.3		14T – 7.3		ns
t_{WHQX}	Data hold after XWR	2T – 3.1		2T + 1.7		ns
t_{RLAZ}	Address float after XRD		0		0	ns
t_{AVSDL}	Address valid to XCSDATA		14.0		12.6	ns
t_{SDLSDH}	XCSDATA pulse width	24T – 0.4		24T – 5.0		ns

(C_L for Port A = 120pF; C_L for XPSEN = 10pF; C_L for all others = 80pF)

Table 6-5: Timing Values for Accessing the Data Memory

Hardware Versions		DPC31 Step C1		DPC31 Step B		
Symbol	Parameter	Min	Max	Min	Max	Unit
t_{LHLL}	ALE pulse width	4T – 4.5		4T – 1.0		ns
t_{AVLL}	Address setup to ALE	2T –9.5		2T – 8.8		ns
t_{LLAX}	Address hold after ALE	2T – 4.3		2T – 9.7		ns
t_{LLIV}	ALE low to valid instr in		8T – 31.6		8T – 31.6	ns
t_{LLPL}	ALE to XPSEN	2T – 3.5		2T – 4.7		ns
t_{PLPH}	XPSEN pulse width	6T + 0.8		6T – 1.5		ns
t_{PLIV}	XPSEN to valid instr in		6T – 27.0		6T – 27.0	ns
t_{PXIX}	Input instruction hold after XPSEN	0		0		ns
t_{PXIZ}	Input instruction float after XPSEN		2T + 4.0		2T + 4.0	ns
t_{AVIV}	Address to valid instr in		10T – 45.6		10T – 45.6	ns
t_{AZPL}	Address float to XPSEN	-0.3		0		ns
t_{PLSCL}	XPSEN to XCSCODE		5.0		18.3	ns
t_{SCLSCH}	XCSCODE pulse width	6T + 1.6		6T – 1.5		ns
t_{SCXIX}	Input instruction hold after XCSCODE	0		0		ns
t_{SCXIZ}	Input instruction float after XCSCODE		2T + 1.9		2T – 14.3	ns

(C_L for Port A = 120pF; C_L for XPSEN = 10pF; C_L for all others = 80pF)

Table 6-6: Timing Values for Accessing the Code Memory

7 SSC Interface (SPI)

Symbol	Hardware Versions Parameter	DPC31 Step C1 min	 max	DPC31 Step B min	 max	Unit
f_{SSCLK}	Operating Frequency		12		12	MHz
t_{CYC}	Cycle Time	83.3		83.3		ns
t_{WH}	Clock High Time	40		40		ns
t_{WL}	Clock Low Time	40		40		ns
t_{SU}	Data Setup Time (Inputs)		28		28	ns
t_H	Data Hold Time (Inputs)	0		0		ns
t_V	Data Valid Time after Enable Edge		2.6		1.0	ns
t_{HO}	Data Hold Time (Outputs, after Enable Edge)	0.1		-1.0		ns

Table 7-1: Timing Values for the SSC Interface

8 Mechanical Specification

8.1 PQFP-100 Casing

Casing Dimensions	DPC31 Step C1			DPC31 Step B Casing supplied			DPC31 Step B specified			Unit
Name	min	nom	max	min	nom	max	min	nom	max	
A	---	3.04	3.40	---	---	3.0	---	---	3.0	mm
A1	0.25	0.33	---	0.0	0.1	0.2	0.050	0.125	0.200	mm
A2	2.57	2.71	2.87	2.6	2.7	2.8	---	2.7	---	mm
D	22.95	23.20	23.45	23.2	23.6	24.0	23.0	23.2	23.4	mm
D1	19.90	20.00	20.10	19.8	20.0	20.2	19.8	20.0	20.2	mm
E	16.95	17.20	17.45	17.2	17.6	18.0	17.0	17.2	17.4	mm
E1	13.90	14.00	14.10	13.8	14.0	14.2	13.8	14.0	14.2	mm
L	0.65	0.70	0.95	0.6	0.8	1.0	0.6	0.8	1.0	mm
e		0.65			0.65			0.65		mm
B	0.22	---	0.38	0.2	0.3	0.4	0.25	0.32	0.40	mm
c	0.13	---	0.23	0.14	0.15	0.20	0.11	0.17	0.22	mm
α	12	---	16		k.A.			k.A.		°
β	0	---	7	0	5	10	0	3	10	°
γ	0	---	---		k.A.			k.A.		°
G	0.13	---	---		k.A.			k.A.		mm
H		1.60 REF.		1.6	1.8	2.0	1.4	1.6	1.8	mm
J	---	0.30	---		k.A.			k.A.		mm
K	0.40	---	---		k.A.			k.A.		mm
2H		3.2			3.6			3.2		mm

Table 2.1.1: Comparison of Casing Measurements

8.2 DPC31 Pinout

Pin	Name	Type	Comment	Pin	Name	Typ	Comment
1	GND	Supply		51	PA_7	In/Out	4mA
2	VDD	Supply		52	VDD	Supply	
3	NTEST1	In		53	GND	Supply	
4	NTEST2	In		54	PB_0	In/Out	4mA
5	TST1	In		55	PB_1	In/Out	4mA
6	RESET	In	Schmitt-Trig.	56	PB_2	In/Out	4mA
7	AGND	Supply		57	PB_3	In/Out	4mA
8	AVDD	Supply		58	PB_4	In/Out	4mA
9	GND	Supply		59	PB_5	In/Out	4mA
10	PE_0	In/Out	8mA	60	PB_6	In/Out	4mA
11	PE_1	In/Out	8mA	61	PB_7	In/Out	4mA
12	PE_2	In/Out	8mA	62	GND	Supply	
13	PE_3	In/Out	8mA	63	PC_0	In/Out	4mA
14	PE_4	In/Out	8mA	64	PC_1	In/Out	4mA
15	PE_5	In/Out	8mA	65	PC_2	In/Out	4mA
16	PE_6	In/Out	8mA	66	PC_3	In/Out	4mA
17	PE_7	In/Out	8mA	67	PC_4	In/Out	4mA
18	PF_0	In/Out	4mA	68	PC_5	In/Out	4mA
19	PF_1	In/Out	4mA	69	PC_6	In/Out	4mA
20	PF_2	In/Out	4mA	70	PC_7	In/Out	4mA
21	PF_3	In/Out	4mA	71	PD_0	In/Out	4mA
22	PF_4	In/Out	4mA	72	PD_1	In/Out	4mA
23	PF_5	In/Out	4mA	73	PD_2	In/Out	4mA
24	PF_6	In/Out	4mA	74	PD_3	In/Out	4mA
25	PF_7	In/Out	4mA	75	PD_4	In/Out	4mA
26	PG_0	In/Out	4mA	76	PD_5	In/Out	4mA
27	PG_1	In/Out	4mA	77	PD_6	In/Out	4mA
28	GND	Supply		78	PD_7	In/Out	4mA
29	VDD	Supply		79	VDD	Supply	
30	PG_2	In/Out	4mA	80	GND	Supply	
31	PG_3	In/Out	4mA	81	$BOOTTYP_0$	In	
32	PG_4	In/Out	4mA	82	$BOOTTYP_1$	In	
33	PG_5	In/Out	4mA	83	DBX	In	
34	PG_6	In/Out	4mA	84	$BUSTYP_0$	In	
35	PG_7	In/Out	4mA	85	$BUSTYP_1$	In	
36	PH_0	In/Out	4mA	86	$BUSTYP_2$	In	
37	PH_1	In/Out	4mA	87	RXD_RXS	In	Schmitt-Trig.
38	PH_2	In/Out	4mA	88	XCTS_RXA	In	Schmitt-Trig.
39	XCSDATA	Out	4mA	89	XPLLEN	In	
40	GND	Supply		90	SSDI	In	
41	XCSCODE	Out	4mA	91	GND	Supply	
42	XPSEN	In/Out	4mA	92	SSCLK	Out	8mA
43	ALE	In/Out	4mA	93	SSDO	Out	8mA
44	PA_0	In/Out	4mA	94	CLKOUT1X4	Out	8mA
45	PA_1	In/Out	4mA	95	TXD_TXS	Out	8mA, **3.3V**
46	PA_2	In/Out	4mA	96	RTS_TXE	Out	8mA, **3.3V**
47	PA_3	In/Out	4mA	97	GND	Supply	
48	PA_4	In/Out	4mA	98	XTAL1_CLK	In	
49	PA_5	In/Out	4mA	99	XTAL2	Out	
50	PA_6	In/Out	4mA	100	CLKOUT1X2	Out	8mA

Table 8-1: Pin Assignment for the QFP-100 Casing (the signals starting with 'X' are low-active)

The driver power has changed for all output drivers in the above Table 2-1.

Hardware Versions Parameter	DPC31 Step C1	DPC31 Step B	Unit
Driver Power	4 8	3 9	mA mA

Note:
Regarding the 5V tolerant 8mA output drivers by Step C1, the current driven by an H-level is higher than for the 9mA output drivers by Step B.