!!!! Current information about using the **SPC4 !!!**

1. In contrast to the description of the SPC4 Version 1.1 dated 12.07.95, the description in chapter 3 PIN assignment is backwards. Pin 24 AS in synchronous operation with Motorola processor must be located at VSS instead of VDD.

2. Access under Lock Chapter 11.3.2, especially in pure DP-Mode, the Tsdr time of the SPC4 is to be included when calculating the max. allowable Lock time. The formula must be Tlock < Tslot - Tsdr where Tsdr, dependent on the baud rate, lies between 60-120 Tbit.

3. Intel X86 asynchronous, the SPC4 is driven with an Intel Prozessor 80286 so, per the Intel description, for example, an 82C284 must be used to process the Ready Signal.
   The 80286 expects a synchronous Ready Signal, however, the SPC4 only delivers an asynchronous Signal.

4. Motorola asynchronous, the SPC4's Signal AS is not to be connected with the processor's AS Signal but rather with the processor's CS Signal.

5. General note which is already mentioned in the documentation but still always leads to incorrect procedure.
   Chapter 11, in few cases read procedures with errors can occur from the internal RAM.
   Solution: The later signal from both RD or CS must maintain a Setup Time of 8ns before the rising edge of the SPC4 pulse.
   If the SPC4 pulse is running asynchronous to the microprocessor's pulse, the RD or the CS signal must be synchronized, for example, with a Flip-Flop.
   With synchronous pulse and concurrence of the rising pulse edge with the RD or CS signal, a inverter in the pulse of the SPC4 is sufficient.