SIEMENS

SIMATIC NET

ASIC
SIM 1-2

Function Manual

Release 02/2007

C79000-G8976-C215-01

Classification of Safety-Related Notices

This document contains notices which you should observe to ensure your own personal safety, as well as to protect the product and connected equipment. These notices are highlighted in the manual by a warning triangle and are marked as follows according to the level of danger:

Danger

indicates that death, severe personal injury **will** result if proper precautions are not taken.

Warning

indicates that death, severe personal injury **can** result if proper precautions are not taken.

Caution

with a warning triangle indicates that minor personal injury can result if proper precautions are not taken.

Caution

without a warning triangle indicates that damage to property can result if proper precautions are not taken.

Notice

indicates that an undesirable result or status can result if the relevant notice is ignored.

Note

highlights important information on the product, using the product, or part of the documentation that is of particular importance and that will be of benefit to the user.

Trademarks

SIMATIC®, SIMATIC NET®, SIMATIC NET Networking for Industry®, SINEC®, SCALANCE® and SINAUT® are registered trademarks of Siemens AG.

Third parties using for their own purposes any other names in this document which refer to trademarks might infringe upon the rights of the trademark owners.

Disclaimer

We have checked the contents of this manual for agreement with the hardware and software described. Since deviations cannot be precluded entirely, we cannot guarantee full agreement. However, the data in this manual are reviewed regularly and any necessary corrections included in subsequent editions. Suggestions for improvement are welcome.

Siemens AG
Automation and Drives
Industrial Communication
Postfach 4848, D-90327 Nürnberg

Safety Instructions Regarding your Product

Before you use the product described here, read the safety instructions below thoroughly.

Qualified Personnel

Only qualified personnel should be allowed to install and work on this equipment . Qualified persons are defined as persons who are authorized to commission, to ground, and to tag circuits, equipment, and systems in accordance with established safety practices and standards.

Correct Usage of Hardware Products

Note the following:

Warning

This device and its components may only be used for the applications described in the catalog or the technical description, and only in connection with devices or components from other manufacturers which have been approved or recommended by Siemens.

This product can only function correctly and safely if it is transported, stored, set up, and installed correctly, and operated and maintained as recommended.

Before you use the supplied sample programs or programs you have written yourself, make certain that no injury to persons nor damage to equipment can result in your plant or process.

EU Directive: Do not start up until you have established that the machine on which you intend to run this component complies with the directive 98/37/EEC.

Correct Usage of Software Products

Note the following:

Warning

This software may only be used for the applications described in the catalog or the technical description, and only in connection with software products, devices or components from other manufacturers which have been approved or recommended by Siemens.

Before you use the supplied sample programs or programs you have written yourself, make certain that no injury to persons nor damage to equipment can result in your plant or process.

Prior to Commissioning

Prior to commissioning, note the following warning:

Caution

Prior to startup read the relevant documentation. For ordering data of the documentation, please refer to catalogs or contact your local Siemens representative.

Preface

Purpose of manual

This manual supports you during the development of a Fieldbus Medium Attachment Unit (MAU) for 31.25 Kbps in compliance with IEC 61158-2 with the SIM 1-2 (**S**iemens **I**EC **M**AU) and a small number of external components.

Which Data Link Layer protocol is implemented is irrelevant. In conjunction with a suitable communication controller, for example SPC 2-4, devices with a fieldbus attachment (supplied with power locally or over the bus) can be implemented with little effort.

This manual serves both as a function manual and as a data sheet for the developer of the electronics.

Aims

With the aid of this manual, you will be able to develop a fieldbus medium attachment unit (MAU) for 31.25 Kbps for your application with little effort using the SIM 1-2.

We assume that you are familiar with the relevant standards and specifications.

Certification

The products and systems listed in this document are manufactured and marketed using a quality management system complying with DIN ISO 9001 and certified by DQS (certificate register no. 2613). The DQS certificate is recognized in all IQNet countries (Reg. No.: 2613).

Contents

Area of Application and Characteristics 1

1.1 Overview

Examples of applications for the SIM 1-2

The SIM 1-2 (**S**iemens **I**EC **M**AU) allows the setting up of a fieldbus **M**edium **A**ttachment **U**nit (MAU) for 31.25 Kbps complying with IEC 61158-2 regardless of the implemented data link layer protocol.

In conjunction with a suitable communication controller, for example, SPC 4-2, devices with a fieldbus attachment can be implemented with little effort.

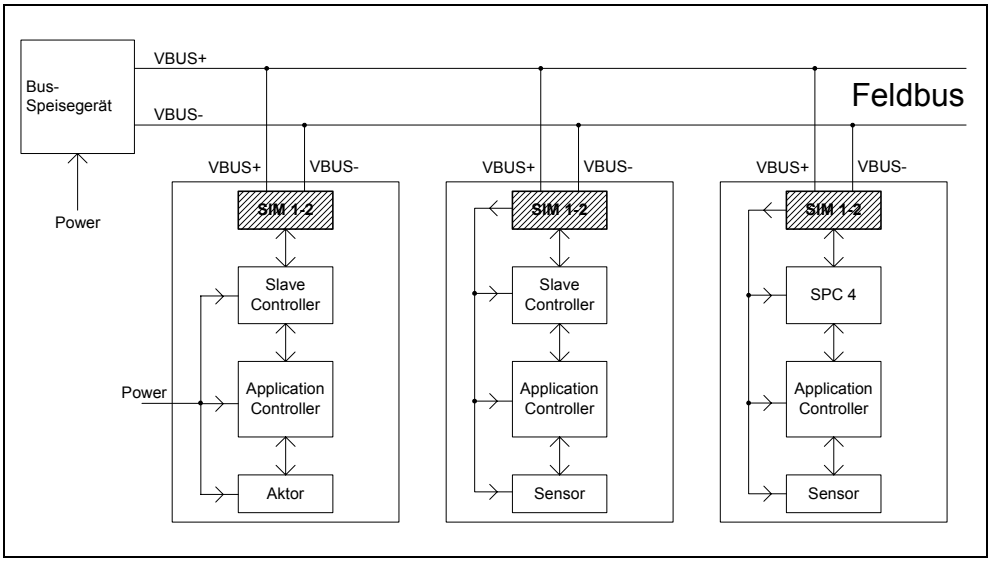
The SIM 1-2 supports all send and receive functions (including jabber control) and the high-impedance decoupling of auxiliary energy from the bus cable.

It provides a selectable, stabilized power supply and also allows the setup of an galvanically isolating power supply with a few passive components.

As an alternative to the standard signal interface (TxS, TxE, RxS, RxA), the ASIC includes special interface logic that provides low power consumption and an easy-to- implement interface for galvanic signal isolation.

Block diagrams of examples

The following diagram illustrates examples of SIM 1-2 applications.



1.2 Essential Characteristics

Description

The essential characteristics of the SIM 1-2 (IEC MAU) are listed below.

Characteristics of fieldbus attachment

Using the SIM 1-2, a fieldbus attachment can be implemented with the following characteristics.

- The SIM 1-2 (IEC MAU) supports fieldbus attachments for 31.25 Kbps in compliance with IEC 6 1158-2.
- The SIM 1-2 can be connected to all Manchester encoders/decoders in compliance with IEC 61158-2.
  As a result, the SIM 1-2 can also be connected to all fieldbus controllers that already include a Manchester encoder/decoder in compliance with IEC 61158 2.
- Jabber inhibit (jabber control prevents a node from transmitting indefinitely on the bus)
- Sender with current modulator for bias currents:
  - Asymmetric modulation from 2 mA to 10 mA
  - Symmetric modulation from 10 to 50 mA

Power-optimized electrical isolation

The SIM 1-2 supports simple and power-minimized galvanic isolation between MAU and user electronics by means of:

- Integrated voltage converter for power-optimized, unregulated voltage transformation; external transformer and rectifier are required.
- Integrated interface logic for simple and current-saving galvanic signal isolation, current consumption in permanent operation < 2 mA; 2 optocouplers and suitable controller interface logic are necessary on the controller.

Properties of the SIM 1-2

- Minimum space required for the MAU interface
- Minimum number of external components
- Little space required due to SMD housing MLPQ 40
- Ambient temperature range -40 to +85 °C
- Low current consumption for own supply
- Bus voltage 9 V to 32 V (functional range)
- Stabilized output voltage for the user:
  - Can be set in the range from 2 V to 5 V (tolerance ±3 %)
  - Up to 50 mA (total) available
- On-chip voltage reference
- On-chip voltage monitoring
- On-chip RESET and PDWN for safe power-up and power down management of connected logic circuits

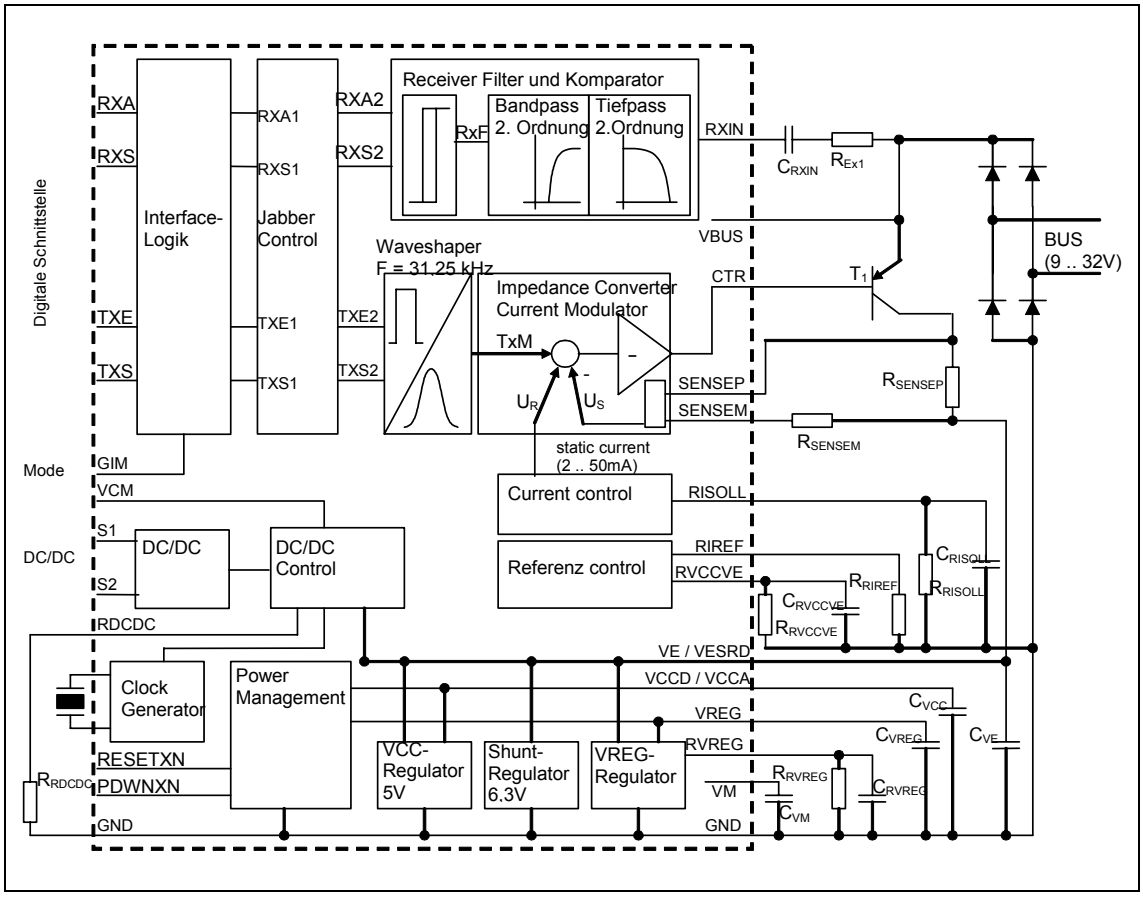
Functional Description of the SIM 1-2

2

2.1 Block Diagram

Description

The following block diagram represents the SIM 1-2 functions as blocks.



2.2 Pin Description

2.2.1 Pin Assignment

Description

The following table describes the assignment of the pin numbers to the symbolic pin names. The table also includes a brief description of the functions.

No.	Name	I/O * 1)	A/D * 2)	Description
1	CTR	O	A	Control output for controlling bus current over T1
2	SENSEP	I/O	A	Actual current sensing for the bus current control and output of the startup bypass
3	SENSEM	I/O	A	Correction of the actual current sensing for the bus current control by taking into account the circulating currents over Pad CTR and VBUS
4	RIREF	I/O	A	Generation of an internal reference current with possible external adjustment
5	RISOLL	I/O	A	Set reference for bus current control (2 mA to 50 mA corresponds to 0.1 MΩ to 2.5 MΩ)
6	RVCCVE	I/O	A	Generation of an internal reference voltage and at the same time measuring point for an external adjustment to RIREF (target : U (RVCCVE) = 1 V)
7	RVREG	I/O	A	Set reference for VREG (2 V to 5 V corresponds to 1.0 MΩ to 2.5 MΩ)
8	GND	P	A	Ground
9	VE	P	A	Regulated supply voltage (6.3 V), derived from U (RVCCVE); regulated only in conjunction with VESRD!
10	VESRD	O	A	Collector of the control transistor of the shunt regulator
11	VREG	P	D	Regulated supply voltage (2 V to 5 V), derived from VE and U (RVREG)
12	GND	P	D	Ground
13	RxS	O	D	Receive signal, output
14	RxA	O	D	Receive activity, output
15	TxE	I	D	Transmit enable, input

Table continued on next page

* 1) I = input, O = output, P = power
* 2) A = analog, D = digital

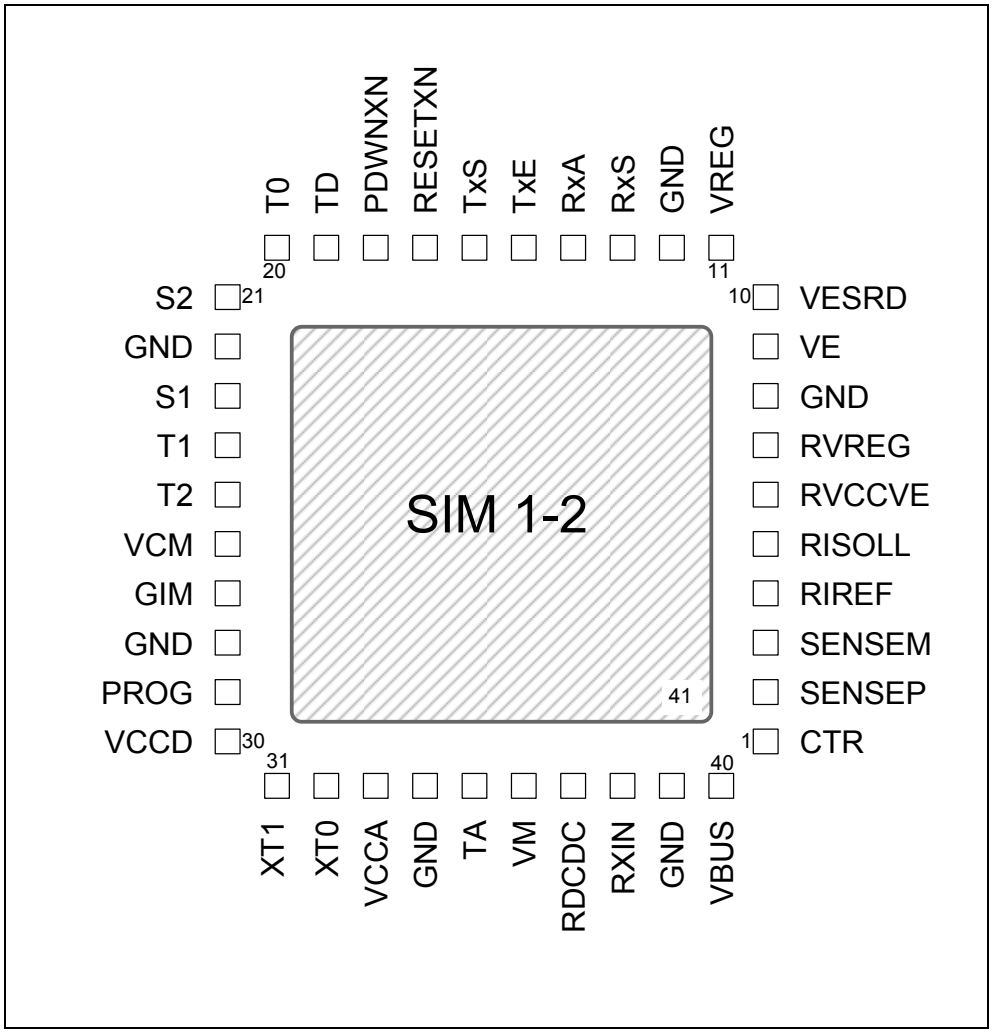
Continued

No.	Name	I/O * 1)	A/D * 2)	Description
16	TxS	I	D	Transmit signal, input
17	RESETXN	O	D	Reset output for external logic supplied by VREG
18	PDWNXN	O	D	Power down – Prewarning signal for external logic supplied by VREG
19	TD			Must be connected to GND.
20	T0			Must be connected to GND.
21	S2	O	D	Switch output 2 of DC/DC converter, open drain
22	GND	P	D	Ground
23	S1	O	D	Switch output 1 of DC/DC converter, open drain
24	t1			Must be connected to GND.
25	T2			Must be connected to GND.
26	VCM	I	D	Voltage converter mode – enabling of DC/DC converter
27	GIM	I	D	Galvanic isolation mode – enabling of power-saving interface
28	GND	P	D	Ground
29	PROG	P	D	Must be connected to VCCD.
30	VCCD	P	D	Regulated supply voltage (5 V) for digital circuit
31	XT1	I/O	D	Quartz or resonator connector, with external clock supply XT1 used as input
32	XT0	I/O	D	Quartz or resonator connector, with external clock supply XT0 is connected to GND
33	VCCA	P	A	Regulated supply voltage (5 V) for analog circuit
34	GND	P	A	Ground
35	TA			Must be connected to GND.
36	VM	O	A	Middle voltage reference (derived from VCCA)
37	RDCDC	I	A	Reference for startup current of the DC/DC converter
38	RXIN	I	A	Input of receiver filter
39	GND	P	A	Ground
40	VBUS	P	A	Connector for supplying the ASIC with the rectified bus voltage
41	GND	P	A/D	Chassis, metal surface below the housing

* 1) I = input, O = output, P = power
* 2) A = analog, D = digital

2.2.2 Pin Arrangement

Pin layout in the 40-pin housing 40LD MLPQ 6x6 VJJD-2



2.3 Basic Functions of the SIM 1-2

The basic functions described in this section are required for the minimum functionality of the SIM 1-2.

2.3.1 Interfacing with the Bus Cable: VBUS and GND

The interfacing to the positive side of the bus system is over VBUS. Externally, at least one diode must be included as polarity reversal protection to avoid both destruction of the ASIC and return feed to the bus cable if a short-circuit occurs.

The interfacing to the negative side of the bus system is over GND.

As an alternative to a diode as polarity reversal protection, a rectifier bridge can be used as polarity reversal protection and feedback protection.

2.3.2 Control Loop: CTR

This output controls the base of the external PNP transistor T1 that supplies the local consumer connected to VE and switches to output signal to the bus by modulating the current consumption.

2.3.3 Current Sensing by SENSEP and SENSEM

The shunt resistor R_{SENSEP} is used to sense the current available as supply current over the collector. The current fed past R_{SENSEP} over VBUS and CRT is sensed by the shunt resistor R_{SENSEM}.

The sum of the two currents corresponds to the current taken from the bus.

2.3.4 Bus Connector

Bus Current Consumption

Using the resistor R_{RISOLL}, the mean current taken from the bus is set from 2 mA to 50 mA. In the range from 2 mA to 10 mA, the SIM 1-2 automatically operates in the asymmetric modulation mode. This means that to transmit, the mean current consumption is raised to 10 mA and then lowered again to the set value.

The set mean bus current must always be at least 1 mA higher than the current transferred to the application over VREG and VE (including DC/DC).

R_{RISOLL} [MΩ] = 0.05 * I_{BUS} [mA]

Conditions for R_{RISOLL}: 100 KΩ ≤ R_{RISOLL} ≤ 2.5 MΩ

the capacitor C_{VE} must be dimensioned in the permitted range according to the pulse load by the application or the DC/DC converter.

Caution 1

To achieve the minimum bus current tolerance of 3 %, resistors with a tolerance of ≤ 0.1 % must be used. As an alternative, the bus current can be matched over R_{RISOLL} (see also tolerance calculation in section 2.3.7, "Reference Circuit RIREF, RVCCVE, RVREG, RISOLL“).

Caution 2

Transistor T1 and its cooling surface must be designed according to the set bus current consumption and the resulting dissipation loss.

Input Impedance

To achieve the impedance of 3 kΩ required by IEC 61158-2 at the bus attachment terminals in conjunction with the transistor PZT3906, the EMC capacitances parallel to the bus connector must be limited as follows:

2 mA < I_{BUS} ≤ 15 mA, C_{EMC} ≤ 500 pF

Starting at an I_{BUS} current of 15 mA, the capacitance of C_{EMC} must be reduced continuously. This results in a curve with the following vertices:

I_{BUS}	C_{EMC}
20 mA	C_{EMC} ≤ 340 pF
30 mA	C_{EMC} ≤ 190 pF
40 mA	C_{EMC} = 0 pF

As of a current of ≥ 40 mA, C_{EMC} remains = 0 pF.

At I_{BUS} currents > 40 mA, the required impedance (at 39 kHz) for bus voltages U_{BUS} < 12 V is not achieved.

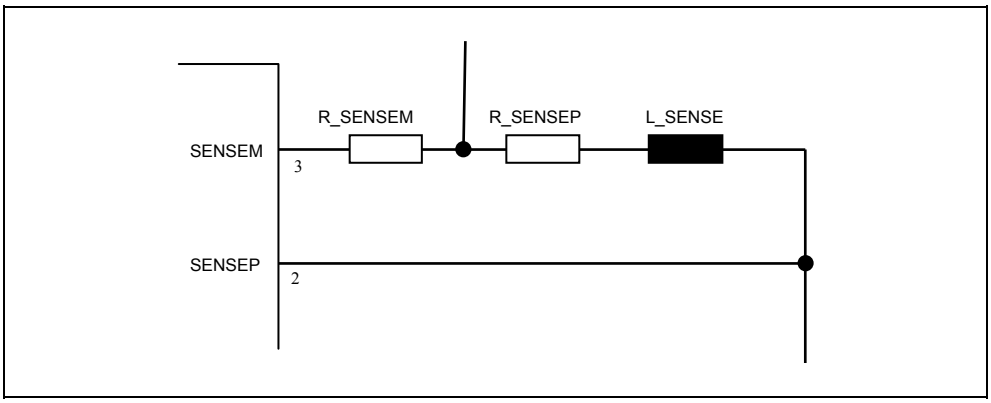
System Stability

We recommend the transistor PZT3906.

If you set the I_{BUS} current to ≥ 30 mA, you should use an additional L_SENSE inductor of 1 µH. This avoids self-excitation and increases system stability.

The L_SENSE inductor is connected in series with R_SENSEP and is not included in the layout proposal in this manual.

As the inductor, we recommend the B82422H from the EPCOS series. If necessary, correct the value of R_SENSEP to achieve the required 10 Ω with the desired accuracy.



2.3.5 Receiver Input: RXIN

The received signal is coupled into the input filter over the external capacitor C_{RXIN} (220 pF) and R_{EX1} (10 kΩ).

2.3.6 Impedance Converter Output/Input: VE/VESRD

These two connectors must be directly connected with each other and then over R_{SENSEP} with the collector of the external transistor T1 and the external energy storage CVE. The voltage at VE/VESRD is regulated to a constant 6.3 V.

2.3.7 Reference Circuit RIREF, RVCCVE, RVREG, RISOLL

Connect the contacts to the specified reference resistors.

Contact	Reference resistor	Meaning
RIREF	R_{RIREF}	All internal references are derived from the current flowing through R_{RIREF}.
RVCCVE	R_{RVCCVE}	R_{RVCCVE} forms the reference for VCC and VE. The RVCCVE pin must be backed up to GND by capacitor C_{RVCCVE}.
RVREG	R_{RVREG}	R_{RVREG} forms the reference for VREG. The RVREG pin must be backed up to GND by capacitor C_{VREG}.
RISOLL	R_{RISOLL}	R_{RISOLL} sets the middle current taken from the bus system.

Notice:

The tolerance of reference resistors is included in the tolerance of the bus current.

You can achieve the minimum tolerance of 3 % with resistors that have a tolerance of ≤ 0.1 %. As an alternative, the bus current can be adjusted over R_{RISOLL}.

Tolerance Calculation

The tolerance of I_{BUS}, V_E and V_{REG} is made up the tolerance of the chip and the tolerance of the reference resistors used R_{RIREF}, R_{RVCCVE}, R_{RVREG}, R_{RISOLL}, R_{SENSEM} and R_{SENSEP}. The precise relationships can be seen in the following formulas.

$$d_{IBUS} = |d_{SIM\ 1\text{-}2}| + |d_{RRISOLL}| + |d_{RRIREF}| + (\beta_{(T1)} / (\beta_{(T1)} + 1)) * |d_{RSENSEP}| + (1 / (\beta_{(T1)} + 1)) * |d_{RSENSEM}|$$

$$d_{VE} = |d_{SIM\ 1\text{-}2}| + |d_{RRVCCVE}| + |d_{RRIREF}|$$

$$d_{VREG} = |d_{SIM\ 1\text{-}2}| + |d_{RRVREG}| + |d_{RRIREF}|$$

The tolerance of the parameters of I_{BUS}, V_E and V_{REG} over the entire temperature range (assuming a circuit with almost ideal reference resistors) is ±3 %; it therefore follows that: $d_{SIM\ 1\text{-}2}$ = ±3 %.

2.3.8 Interface and Application Voltage VREG

With VREG, there is an operating voltage regulated by R_{RVREG} in the range from 2 V to 5 V for local loads. This is also the power supply for the outputs and inputs of the digital interface (TXE, TXS, RXA, RXS, RESETXN, PDWNXN).

2.3.9 Internal Power Supply: VCCD/VCCA, VM

The two pins VCCD and VCCA must be connected directly with each other and backed up to GND over the capacitor C_{VCC}.

No power for local loads may be taken from the internal power supply VCC.

The VM pin must be backed up to GND by capacitor C_{VM}.

2.3.10 Oscillator: XT0, XT1

Pins XT0 and XT1 are provided for the connection of a 2 MHz quartz/ceramic oscillator. Further external components (capacitances) are required depending on the quartz/ceramic oscillator used. With external clock supply, XT0 is connected to GND and XT1 is used as an input.

XT0 and XT1 may each be loaded with a capacitance of ≤ 47 pF.

2.3.11 Digital Interface: TXE, TXS, RXA, RXS

Possible interconnection between the external interface circuit, for example SPC 4-2, and the SIM 1-2:

- Direct connection of TXE, TXS, RXA, RXS with the digital input and output drivers of an external communication controller for the external application electronics.
- Connection of TXE, TXS, RXA, RXS with the digital input and output drivers of an external communication controller galvanically isolated over optocouplers for the external application electronics.
- Interfacing using the power-saving galvanic signal isolation over two optocouplers TXS and RXS.

2.3.12 Test and Manufacturing Pins: TD, T0, T1, T2, TA

For the SIM 1-2 to function perfectly, the test and manufacturing pins TD, T0, T1, T2, and TA must be connected to GND.

2.3.13 Mode Setting GIM and VCM

Galvanic Isolation Mode (GIM)

This input is used to activate or deactivate the power-saving interface to the application.

GIM	Meaning
High	The power-saving pulse duration modulation is used both for the inputs (demodulator on TXS) and for the output (modulator on RXS).
Low	The power-saving pulse duration modulation is not active.

Voltage Converter Mode (VCM)

This input is used to activate or deactivate the DC/DC converter controller.

VCM	Meaning
High	The DC/DC converter is active and controls the outputs S1, S2.
Low	The DC/DC converter is disabled, the outputs S1, S2 are switched with high impedance.

2.3.14 Voltage Monitoring

Voltage Monitor

The voltage monitor monitors the internally generated voltages VE, VCC and VREG.

RESETXN pin

At the RESETXN pin, the SIM 1-2 signals the end of the startup phase with a change from low to high. This means that all required power supplies have reached their desired value.

If the VREG voltage sinks below 90 % of the desired value $VREG_{SOLL}$, a change from high to low at the RESETXN pin signals the reset status of the chip.

PDWNXN pin

At the PDWNXN pin, the SIM 1-2 signals an interruption of the bus supply with a short low pulse. Controlled by this signal, the connected application can initiate a power down sequence.

If the VE voltage sinks below 90 % of the desired value VE_{SOLL}, the prewarning PDWNXN (PDWNXN changes to logic '0' for 10 µs) is output. Communication over TxE, TxS, RxA and RxS is not affected by this.

2.4 Power Supply of the Application

For the power supply of the external application electronics, it is only ever possible to take as much energy as is taken on average from the bus system less the power consumption of the SIM 1-2 itself.

2.4.1 Power Supply VREG

The V_{REG} voltage that can be set between 2 V and 5 V regulated by R_{RVREG} is available as a non-floating power supply for the external application electronics. The V_{REG} power supply can be subjected to a maximum load of 50 mA.

R_{RVREG} [MΩ] = 0.5 * VREG [V]

Conditions for R_{VREG}: 1 MΩ <= R_{VREG} ≤ 2.5 MΩ

Notice:

You achieve the minimum VREG tolerance of 3 % if you use a resistor with a tolerance of ≤ 0,1 % for R_{RVREG} (see also the tolerance calculation in section 2.3.7, "Reference Circuit RIREF, RVCCVE, RVREG, RISOLL“).

2.4.2 Power Supply VE

Caution

The VE voltage of 6.3 V generated by the shunt regulator cannot be used immediately after turning on the power supply of the external application electronics since this can disrupt the startup of the SIM 1-2 considerably.

On completion of the startup phase (indicated by RESETXN), the VE voltage can be used to supply the external application electronics. It is, however, important to make sure that the VE never falls below 80% as a result of sudden load changes.

If the VE voltage sinks below 90% of VE_{SOLL}, a prewarning PDWNXN (low-active) is output (PDWNXN changes to logic '0' for 10 µs). Communication over TxE, TxS, RxA and RxS is not affected by this.

If the VE voltage falls below 80% of VE_{SOLL}, the DC/DC converter and the VREG regulator are turned off. They start again only when VE has reached 92 % again.

When using C_{VE} backup capacitors higher than 33 µF, it is advisable to connect a 1 Ω resistor in series with the capacitor C_{VE} to minimize the risk of superimposing oscillations on the VE power supply.

2.4.3 DC/DC Converters S1 and S2

These outputs are switches for setting up a DC/DC converter. By connecting a transformer, a push-pull transformer for the power supply of a non-floating load can be implemented. Two stages of the DC/DC converter start up as soon as a stable VE supply voltage is present: in other words, before RESET becomes inactive.

To ensure that the VE supply voltage does not break down when the push-pull transformer is starting up (depending on the backup capacitance C_{VE} and the set bus current), the startup takes several stages. The result of startup depends largely on the load on the secondary side. It switches to normal operation after 20 ms with the bridge branches then only functioning as switches. If the voltage at VE sinks below 80% of its desired value due to the load, the startup is repeated from the beginning.

The voltage at the open circuit breaker achieves twice the voltage of VE due to center tapped transformer connected downstream. Moreover, the energy stored in the leakage inductance of the transformer can induce brief voltage peaks when switching the transistor bridge (circuit breaker) that are far higher than twice the value of VE and therefore destroy the circuit breaker. To prevent this, the voltage is limited internally to approximately 20 V. The ability of this voltage limitation to absorb is, however, limited to the energy stored in a leakage inductance of 15 µH. When using a transformer with a leakage inductance of 15 µH to 70 µH, an additional protective circuit must be use to limit the voltage to $2xVE < U_{S1,S2} << 20$ V. A protective circuit between VE and the circuit breakers S1 and S2, each consisting of BAT45 and BZX84C7V5 connected in series.

- Transformers with a leakage inductance up to 15 µH can be activated at S1 and S2 without any further protective circuit.
- Transformers with a leakage inductance up to 70 µH can only be activated at S1 and S2 with additional protective circuits (see section 4.4, „Circuit Examples“).
- Transformers with a leakage inductance > 70 µH cannot be used.

The effective capacitive load on the secondary side during startup (C_{DCDC}) should not exceed 22 µF at I_{BUS} = 50 mA and 4.7 µF at I_{BUS} = 8 mA (see section 2.4.4, ""“).

When using the DC/DC converter on S1 and S2. a minimum current $I_{BUS} \geq 8$ mA is recommended.

2.4.4 Dimensioning the Backup Capacitor

To allow a correct startup behavior, the set constant current consumption and the backup capacitors C_{VE} and C_{DCDC} must be matched up.

Secondary capacitor C_{DCDC}
The dimensions of the secondary capacitor of transformer C_{DCDC} must not be too large depending on the constant current:
C_{DCDC} < IBUS * 0.5 µF/mA

Capacitor C_{VE}
The following applies to capacitor C_{VE}:
$C_{VE} > 2 * Ü * C_{DCDC}$ where $Ü = V_{DCDC}/VE$

Capacitor C_{VREG}
The following applies for capacitor C_{VREG}:
$C_{VREG} \leq 47$ µF

2.5 Internal Functions

2.5.1 Impedance Converter

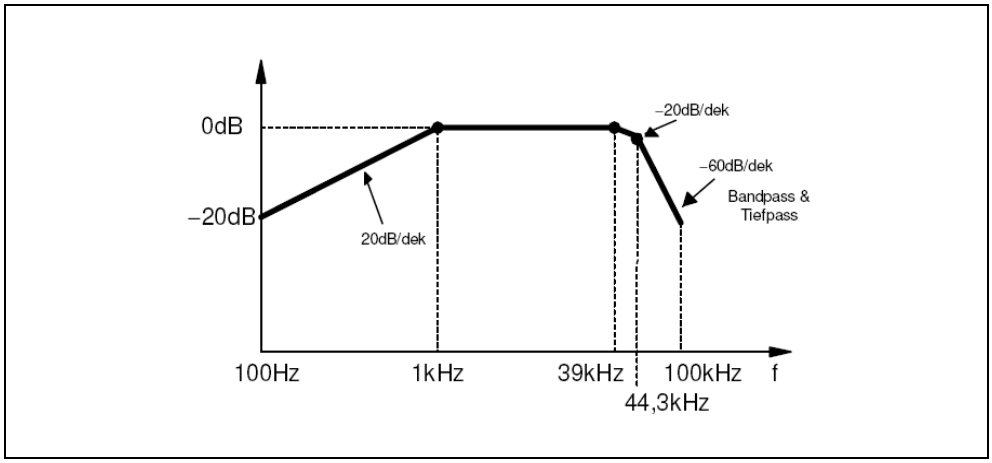
The impedance converter/current modulator and current control function units together along with a few external components and the internal shunt regulator form the high-impedance decoupling of the auxiliary power from the bus cable.

2.5.2 Shunt Regulator

The shunt regulator derives a stabilized voltage VE from the constant current. The part of the total current not required by external loads is diverted to GND. The load current can be taken in any proportions from the power supplies VREG and the DC/DC converter (external transformer necessary).

2.5.3 Signal Filter

The combined input high pass, band pass and low pass filter suppresses disturbances outside of the signal transmission range from 7 kHz to 40 kHz. The band pass and low pass filter is implemented as a switched capacity filter. The input high pass filter is made up of R_{EX1} and C_{RXIN}.



2.5.4 Comparator, Carrier Detector

From the filtered received signal RxF, the comparator forms a logic signal RxS2 suitable for further processing. A carrier detector also monitors the received signal and generates the carrier detect signal RxA2 dependent on the signal amplitude.

2.5.5 Jabber Control

If a node is malfunctioning so that it constantly tries to transmit data via the bus connection (MAU), the data flow must be interrupted to avoid the malfunctioning node for blocking the transmission medium (jabber inhibit). The SIM 1-2 meets the standard IEC 61158-2.

It specifies that transmission of a message to the medium will be interrupted if the message duration exceeds a time of 120 to 240 ms. At the same time, the transmission of the RxS1 data and the RxA1 signal to the node must be inhibited.

After a time of 3 s ± 50% the inhibit is canceled and monitoring the duration of an existing message is restarted.

If the malfunction on the node persists, cancellation of the inhibit be repeated periodically every 3 s ± 50%. Monitoring cannot be disabled.

2.5.6 Wave Shaper

From the logic signals TxS2 and TxE2, the wave shaper generates the analog signal TxM with which the IBUS current is modulated.

2.5.7 Interface Logic

The interface logic forms the interface to the communication controller of the user electronics. Three operating modes are possible:

Without galvanic isolation
If galvanic isolation of the bus interface (MAU) from the application-specific electronics is not required, the send or received signals with GIM = L on the interface are passed on without any processing and switched through to the user electronics. The output level of RxA and RxS is adapted over the interface and application voltage VREG.

Conventional isolation with optocouplers
To achieve galvanic isolation of the lines for data and associated signals, various isolating components and circuits can be used. One common method is to provide an optocoupler for each of the signals TxS, TxE, RxS and RxA.

Power-saving isolation with optocouplers
The SIM 1-2 also provides the option of a power-saving galvanic isolation with only 2 optocouplers.

Technical Specifications

3

This section contains the technical specifications of the SIM 1-2.

3.1 Limit Values

Description

The following table lists the limit values of the SIM 1-2 that must not be exceeded!

Caution

These maximum operating conditions must not be exceeded under any circumstances, otherwise the SIM 1-2 may be destroyed. All voltages relate to GND. A current flowing out of a pin is preceded by a negative sign.

Values for bus interfacing

Name/pin	Parameters	Min	Max	Unit	Remark
VBUS	Supply voltage	-0.3	35.0	V	
SENSEP, SENSEM, CTR, RXIN	Voltage at the inputs and outputs	-0.3	VBUS +0.3	V	RXIN over R_{EX1} and CTR
I (CTR)	Control current at base of T1	-5	5	mA	

Values for supply VE

Name/pin	Parameters	Min	Max	Unit	Remark
VE	Supply voltage	-0.3	7.0	V	
I (VE)	Load current		60	mA	
RIREF, RVCCVE, RVREG, RISOLL	Voltage at the inputs and outputs	-0.3	VE +0.3	V	

Values for supply VCC

Name/pin	Parameters	Min	Max	Unit	Remark
VCCA, VCCD	Supply voltage	-0.3	7.0	V	
I (VCCA) + I (VCCD)	Load current	-2	50	mA	Maximum is peak value if a short occurs (flows over VCCA)
VM, TEST1, TEST2, RDCDC, GIM, VCM, XT0, XT1	Voltage at the inputs and outputs	-0.3	VCCA +0.3 or VCCD +0.3	V	

Values for supply VREG

Name/pin	Parameters	Min	Max	Unit	Remark
VREG	Supply voltage	-0.3	7.0	V	
I (VREG)	Load current	-55	300	mA	The maximum is the peak value if a short circuit occurs.
TxE, TxS, RxA, RxS, PDWMXN, RESETXN	Voltage at the inputs and outputs	-0.3	VREG +0.3	V	
I (RxA), I (RxS)	Load current	-2	16	mA	I_{OH}, I_{OL}
I (PDWMXN), I (RESETXN)	Load current	-1	5	mA	I_{OH}, I_{OL}

Values for DC/DC activation

Name/pin	Parameters	Min	Max	Unit	Remark
S1, S2	Voltage at the outputs	-0.3	20.0	V	Internal terminal voltage (with current limitation!)
I (S1), I (S2)	Load current considered as mean		40	mA	

Values for environmental influences and processing

Name/pin	Parameters	Min	Max	Unit	Remark
T_{OP}	Ambient temperature	-40	85	°C	
T_{STG}	Storage temperature	-55	150	°C	
T_J	Junction operating temperature		135 (preliminary)	°C	Operating junction Temperature
$R_{th\ j\text{-}a}$	Heat transfer resistance junction/environment		26	K/W	Thermal resistance from junction to ambient in free air
Housing	Solder profile		Pb free		JEDEC J-STD-020C
Housing	Solder temperature		260	°C	JEDEC J-STD-020C
Housing	Moisture sensitivity level I		MSL 3		JEDEC J-STD-020C
All pins	Lead finish		Sn		Pb free
All pins	ESD resistance	-1	+1	kV	Human body model

3.2 Normal Operating Conditions and Characteristic Data

Note

The following tables list the normal operating conditions and characteristic data of the SIM 1-2 and are structured according to the corresponding power supply.

The information covers the spread of values that must be kept to at a bus voltage VBUS of 9 V to 32 V and an ambient temperature of –40 °C to 85 °C.

All voltages relate to GND.

A current flowing out of a pin is preceded by a negative sign.

Values for bus interfacing

Name/pin	Parameters	Min	Typ.	Max	Unit	Remark
V_{BUS}	Bus voltage	9.0		32.0	V	Not applied directly to SIM 1-2.
I_{BUS}	Static minimum bus current	1,94	2	2,06	mA	Tolerance +/-3 %
I_{BUS}	Static maximum bus current	48,5	50	51,5	mA	Tolerance +/-3 %
I_{MPP}	Modulation current	16.0	17.5	19.0	mA	Peak-to-peak value
I (VBUS)	Input current at VBUS pin	0.4	0.55	0.75	mA	Bypass current
$I_{VBUSBYPASS}$	Own current requirements startup bypass			40	µA	Own power requirements VBUS
SENSEP, SENSEM	Voltage at SENSEP and SENSEM			7.5	V	
I (SENSEP)	Current SENSEP pin	-0.75			mA	Bypass current
I (SENSEM)	Current SENSEM pin			0.6	mA	Compensation current
R_{SENSEP}, R_{SENSEM}	Actual current value detection		10		Ω	0.1 % tolerance and TK < 15 ppm/K, to achieve 3 % tolerance of the circuit
CTR	Control voltage at base of T1	0		32	V	
I (CTR)	Control current at base of T1	0		0.5	mA	
RXIN	Voltage at RXIN	0		32	V	
RI (RXIN)	Input resistance of the input stage	100k			Ω	Minimum input resistance of the receiver stage

Values for supply VE

Name/pin	Parameters	Min	Typ.	Max	Unit	Remark
VE, VESRD	Voltage at shunt regulator	6,111	6,3	6,489	V	Tolerance +/-3 %
PDWNXN	Prewarning threshold for PDWNXN		0.9 * VE_{SOLL}		V	
RESETXN	Reset threshold for RESETXN		0.9 * $VREG_{SOLL}$		V	
I (VE)	Own current requirements entire SIM 1-2			860	µA	DC/DC function deactivated.
I (VESRD)	Load current at shunt regulator			52.5	mA	Considered as mean
C_{VE}	Capacitance at VE	4.7 -10 %		100 +10 %	µF	Tantalum *1) TAJA475K016R, TAJC107K010R
R_{RIREF}	Reference current generation		1.5		MΩ	*2)
R_{RVCCVE}	Reference voltage generation for VCC and VE		1.0		MΩ	*2)
R_{RVREG}	Reference voltage generation for minimum value V_{REG} = 2 V		1.0		MΩ	*2)
R_{RVREG}	Reference voltage generation for maximum value V_{REG} = 5 V		2.5		MΩ	*2)
R_{RISOLL}	Bus current setting for minimum value I_{BUS} = 2 mA		100		kΩ	*2)
R_{RISOLL}	Bus current setting for maximum value I_{BUS} = 50 mA		2.5		MΩ	*2)
C_{RVCCVE}	Capacitance	9	10	11	nF	Ceramic 6.3 V
C_{RVREG}	Capacitance	42.3	47	51.7	nF	Ceramic 6.3 V
C_{RISOLL}	Capacitance	29.7	33	36.3	nF	Ceramic 6.3 V

*1) At C_{VE} > 33 µF, it is recommended that a 1 Ω resistor is connected in series with C_{VE}.

*2) 0.1 % tolerance and TK < 15 ppm/K, to achieve 3 % tolerance of the circuit.

Name/pin	Parameters	Min	Typ.	Max	Unit	Remark
VCCA, VCCD	Supply voltage VCC	4.75	5.0	5.25	V	Only used internally.
C_{VCC}	Capacitance at VCC pin	0.9		3,63	µF	Tantalum TAJA105K016R, TAJA335K016R
VM	Middle voltage		0.5 * VCCA		V	
C_{VM}	Capacitance at VM pin	90	100	110	nF	Ceramic 6.3 V
XT0. XT1	Clock generation 2 MHz	1.99	2.0	2.01	MHz	Tolerance +/0.5 % (plus the vendor-specific initial tolerance for the typical value)
XT0. XT1	Voltage at XT0 and XT1	-0.3		VCCA +0.3	V	
C_{XT0}, C_{XT1}	Load capacitance	10		47	pF	
VCM, GIM	Input signal high	4.0			V	
VCM, GIM	Input signal low			1.0	V	
VCM, GIM	Input signal hysteresis	0.5			V	
VCM, GIM	Input current			$\pm$10	µA	VIN = GND to VCCD

Values for supply VREG

Name/pin	Parameters	Min	Typ.	Max	Unit	Remark
VREG	Desired voltage at VREG = 2 V	1,94	2	2,06	V	Tolerance +/-3 %
VREG	Desired voltage at VREG = 5 V	4,85	5	5,15	V	Tolerance +/-3 %
I (VREG)	Load current	0		50	mA	
C_{VREG}	Capacitance at VREG pin	4.7 -10 %		22 +10 %	µF	Tantalum TAJA475K016R, TAJA226K016R

Values for DC/DC activation

Name/pin	Parameters	Min	Typ.	Max	Unit	Remark
S1, S2	Terminal voltage S1 and S2 (see section 2.4.3)	2 * VE			V	Internally or externally limited
I (S1), I (S2)	Load current considered as mean			40	mA	
R_{DSON}	R_{DSON} of switches S1 and S2	1.5		8	Ω	Per switch

Values for Communication Interface

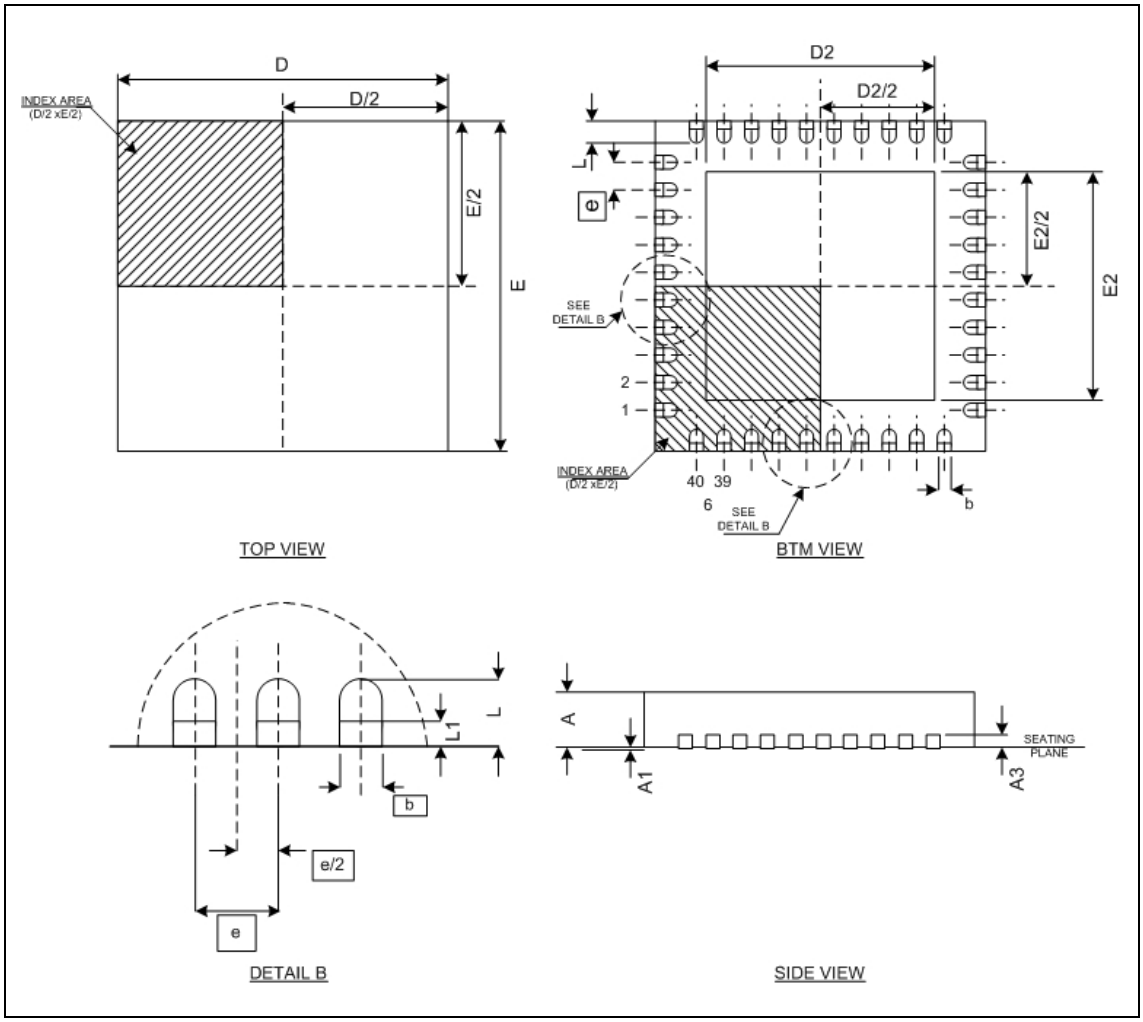
Name/pin	Parameters	Min	Typ.	Max	Unit	Remark
RESETXN, PDWNXN	Output signal VOH	0.8 * VREG			V	I_{OH} = -1 mA
RESETXN, PDWNXN	Output signal VOL			0.4	V	I_{OL} = 5 mA
RxA, RxS	Output signal VOH	VREG -0.1			V	I_{OH} = -0.1 mA
RxA, RxS	Output signal VOH	VREG -0.5			V	I_{OH} = -0.8 mA
RxA, RxS	Output signal VOL			0.1	V	I_{OL} = 0.1 mA
RxA, RxS	Output signal VOL			0.4	V	• If I_{OL} = 10 mA and VREG 3 V to 5 V • If I_{OL} = 4 mA and VREG 2 V to 3 V
TxE, TxS	Input signal VH	0.65 * VREG			V	GIM = GND
TxE, TxS	Input signal VL			0.35 * VREG	V	GIM = GND
TxE, TxS	Input signal VHYST	0.1		0.3 * VREG	V	
TxE, TxS	Input current			±10	µA	VIN = GND to VREG

Values for environmental influences

Name/pin	Parameters	Min	Typ.	Max	Unit	Remark
T_{OP}	Ambient temperature	-40		85	°C	In operation

3.3 Housing MLPQ 40

Drawing of the Housing



Housing Dimensions

The following table lists the dimensions of the housing in millimeters.

Meaning	Min.	Typical	Max.
A	0.8	0.9	1.0
A1	0	0.02	0.05
A3		0.2	
D		6.0	
D2	4.0	4.15	4.25
I		6.0	
E2	4.0	4.15	4.25
e		0.5	
L	0.3	0.4	0.5
L1	0.03		0.15
b	0.18	0.25	0.30

Manufacturing Notes

Caution 1

The **ESD protection measures** must always be adhered to for all electronic components.

Caution 2

The **SIM 1-2** is a **component at risk of cracking** that must be handled as such.

- Before processing the SIM 1-2, it must be subjected to a drying process if the chip has been stored for more than 168 hours without being dry packed (according to JEDEC J-STD-020C Moisture Sensitivity Level 3).
- The component must then by dried at 125 °C for 24 hours and processed within 48 hours. This drying may only be performed once due to the solderability of the component (according to JEDEC J-STD-020C Moisture Sensitivity Level 3).
- The SIM 1-2 is approved for infrared reflow with the lead-free reflow profile according to JEDEC JSTD-020C.
- The lead-free infrared reflow process must not exceed a maximum temperature of 260 °C on the surface of the package and may be 260 °C for only three seconds. Over a period of maximum 150 seconds, the temperature of the package surface may exceed 217 °C (according JEDEC J-STD-020C).
- Lead finish: Sn

Application Examples 4

4.1 Interface Logic

4.1.1 Overview of the Interface to the Communication Controller

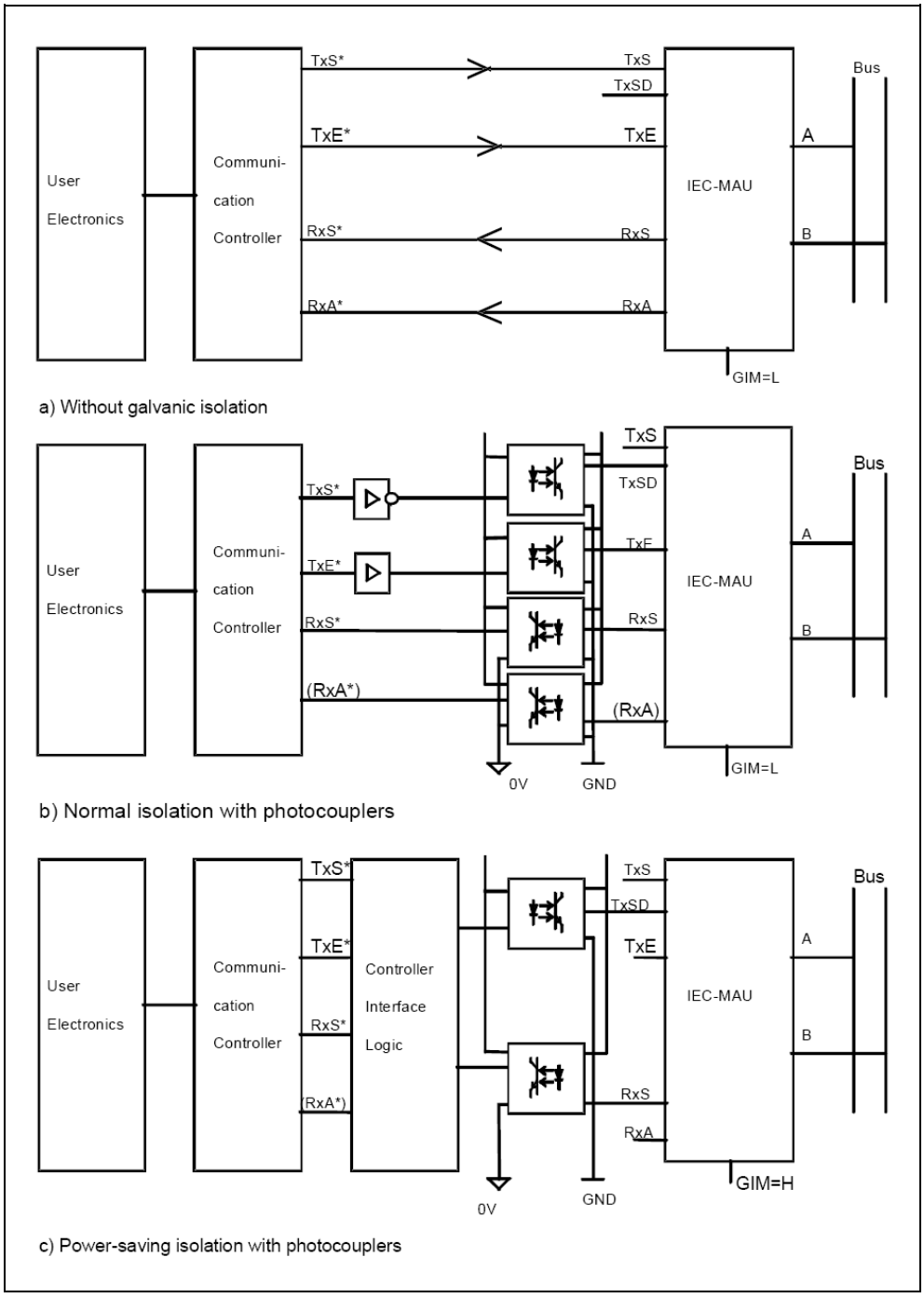
The interface logic forms the interface to the communication controller of the user electronics. As shown in the following diagram, three modes are possible.

- **Without galvanic isolation**
  If galvanic isolation of the bus interface (SIM1-2) from the application-specific electronics is not required, the send or received signals are passed on without any processing and switched through to the user electronics. (Figure a). The output level of RxA and RxS is adapted over the output voltage VREG as reference voltage.

- **Conventional isolation with optocouplers**
  To achieve galvanic isolation of the lines for data and associated signals, various isolating components and circuits can be used. The conventional method is a separate optocoupler each for the signals TxS, TxE, RxS and RxA (Figure b).

- **Power-saving isolation**
  With the power-saving galvanic isolation, only two optocouplers are necessary, the data is then transferred using pulse duration modulated signals in the galvanic isolation mode (Figure c). The Galvanic Isolation Mode (GIM) is enabled with GIM = H.

  The send and receive functions are implemented separately so that if the physical characteristics of the bus are correct, the frame sent over TXS can be received over RXS. The following two sections explain this circuit in more detail.


User
Electronics
Communi-
cation
Controller
TxS*
TxE*
RxS*
RxA*
TxS
TxSD
TxE
RxS
RxA
IEC-MAU
Bus
A
B
GIM=L
a) Without galvanic isolation
User
Electronics
Communi-
cation
Controller
TxS*
TxE*
RxS*
(RxA*)
TxS
TxSD
TxE
RxS
(RxA)
IEC-MAU
Bus
A
B
0V
GND
GIM=L
b) Normal isolation with photocouplers
User
Electronics
Communi-
cation
Controller
TxS*
TxE*
RxS*
(RxA*)
Controller
Interface
Logic
TxS
TxSD
TxE
RxS
RxA
IEC-MAU
Bus
A
B
0V
GND
GIM=H
c) Power-saving isolation with photocouplers

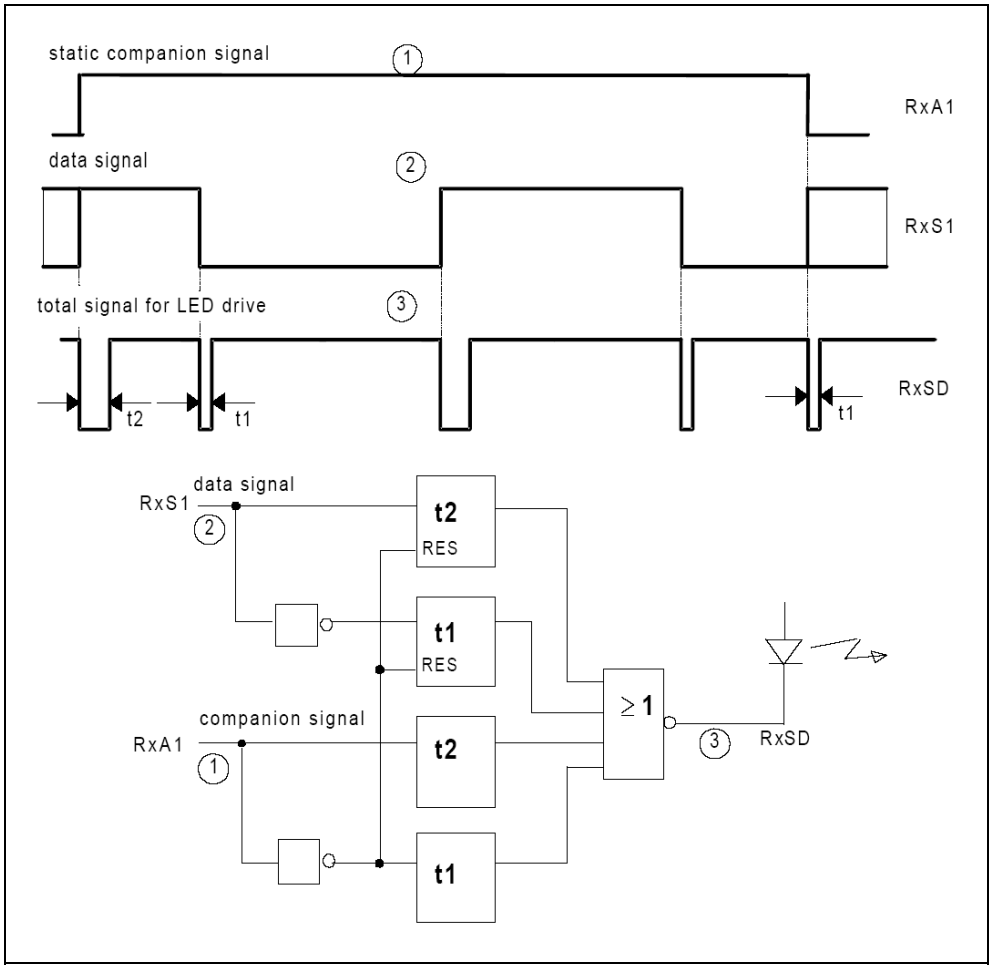
4.2 Power-saving Isolation with Optocouplers

4.2.1 Internal Pulse Duration Modulator

Description of the Signal Shaping in the Modulator

In Galvanic Isolation Mode (GIM = H), the PD modulator converts the serial signal to be transferred into a duration modulated pulse train in which the rising edge of the send signal is assigned a long pulse and the falling edge a short pulse. A long and a short pulse are also generated with the edges of the static associated signal and added to the pulse train of the data signal. The total signal generated in this way is used to drive the LED of an optocoupler.

Design Example



4.2.2 Internal Pulse Duration Demodulator

Description of the Input Evaluation

In Galvanic Isolation Mode (GIM=H) the wanted signal for the PD demodulator is obtained from the collector signal of the optocoupler transistor using a comparator.

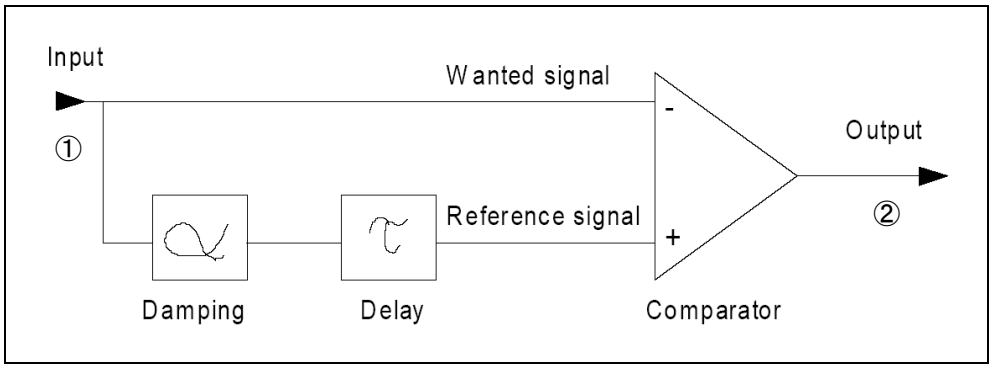
The signal transitions (especially during operation with low currents) behave differently over time depending on the characteristics of the optocoupler itself and its circuitry.

Evaluation with a fixed discriminator threshold on the comparator leads to different delays of the edges causing unacceptable signal distortions. It is possible to minimize the distortion if the when the switching times of the comparator are close to the beginning of the signal changes.

This, however, requires different switching thresholds dependent on the edge or signal directions. A suitable adaptation of the switching threshold can be implemented if this is derived from the wanted signal itself.

The principle behind this dynamic input signal evaluation is shown in the figure below. At the same time, the reference signal of a comparator is obtained from the wanted signal over a damping element a and a delay element.

Circuit Principle of Input Evaluation



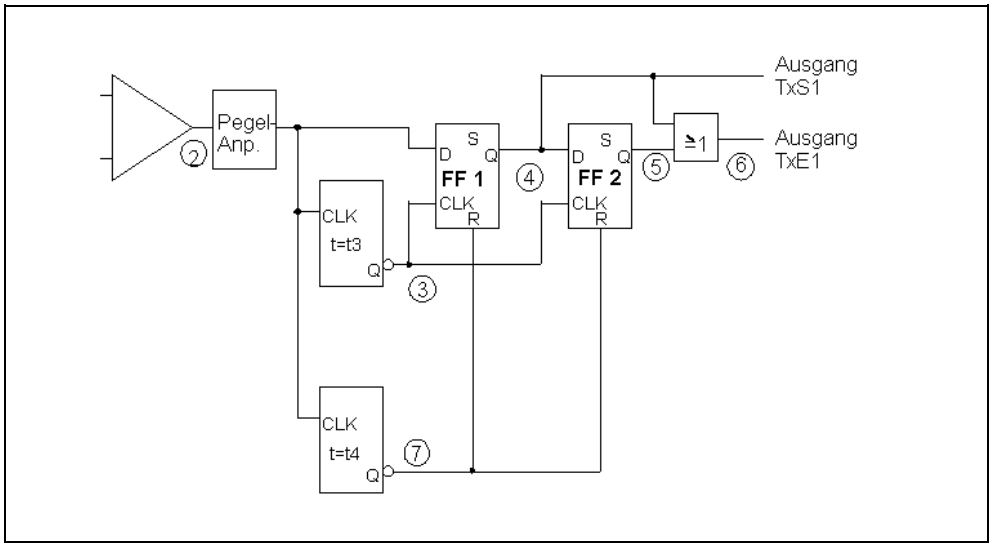
Description of the Signal Evaluation

The leading edge on an incoming pulse ② triggers a time stage with a run time of t3. The following time condition applies: $t1 < t3 < t2$.

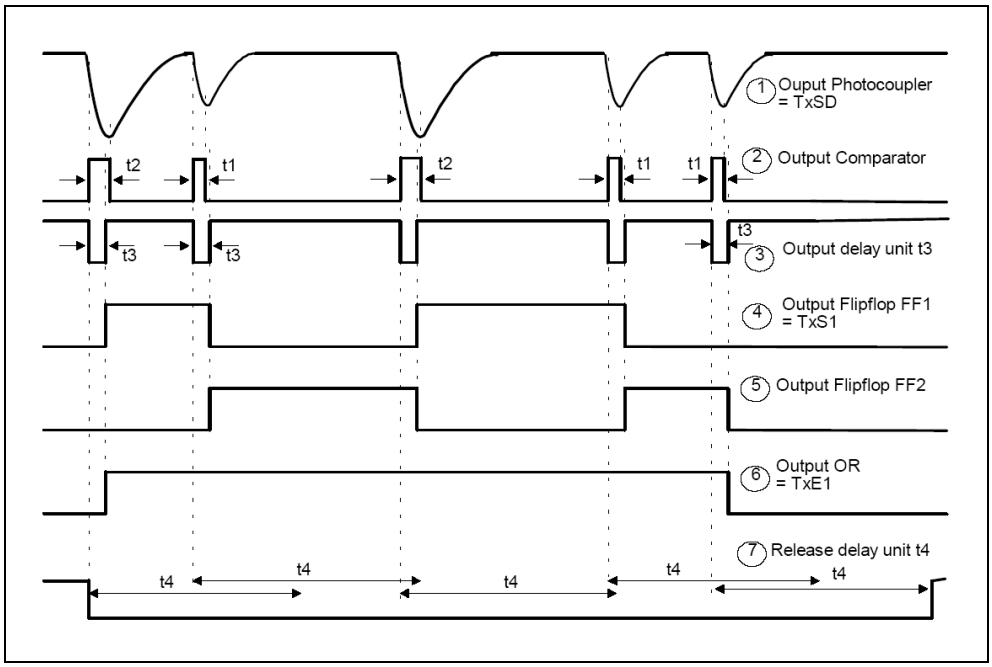
On expiry of t3, a scan for pulse length t1 or t2 is performed. Depending on the detected pulse length t1 or t2, the flip-flop FF 1 is set to L or H. The output of the flip-flop therefore corresponds to the serial data signal ④. The output signal ⑤ of a further flip-flop FF 2 is ORed with signal ④. If two short pulses occur one after the other, both flip-flops are reset. The OR operation results in an L, which is detected as the end of the static signal ⑥. A further triggerable delay element t4 (40 *s * t4 * 100 µ*s) resets both evaluation flip-flops with the signal ⑦ in transmission pauses to suppress undefined signals being set as a result of noise.

Pulses < 0.5 *s at the comparator output will be suppressed reliably, pulses * 1 µs will be reliably detected.

Principle of Demodulator Signal Evaluation



Signal Evaluation in the Demodulator



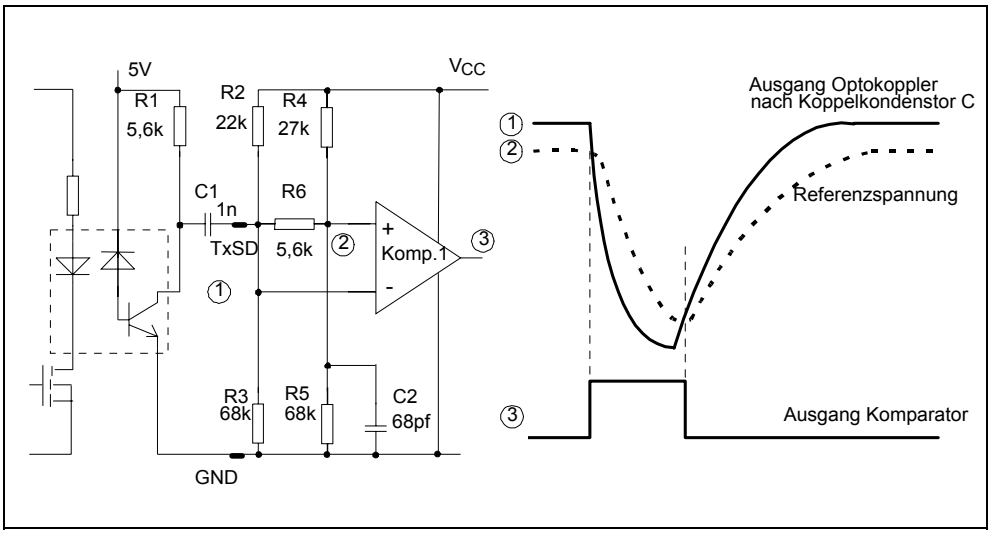
4.2.3 External Dynamic Signal Evaluation

Description of the Dynamic Input Evaluation

The circuit below is an example of retrieving the useful signal from the collector signal of the optocoupler transistor for the downstream communication controller in galvanic isolation mode.

The two voltage dividers R2/R3 and R4/R5 move the working range of the comparator to the middle of the SPC-4–2 supply voltage V_{CC}. The difference between the values of R2 and R4 results in an offset in the quiescent state. R6 brings about a reduction in amplitude and C2 a delay of the reference voltage in the active state. The capacitor C1 decouples the supply voltage of the optocoupler from the communication controller supply voltage $V_{CC.}$

Example of Demodulator Input Evaluation

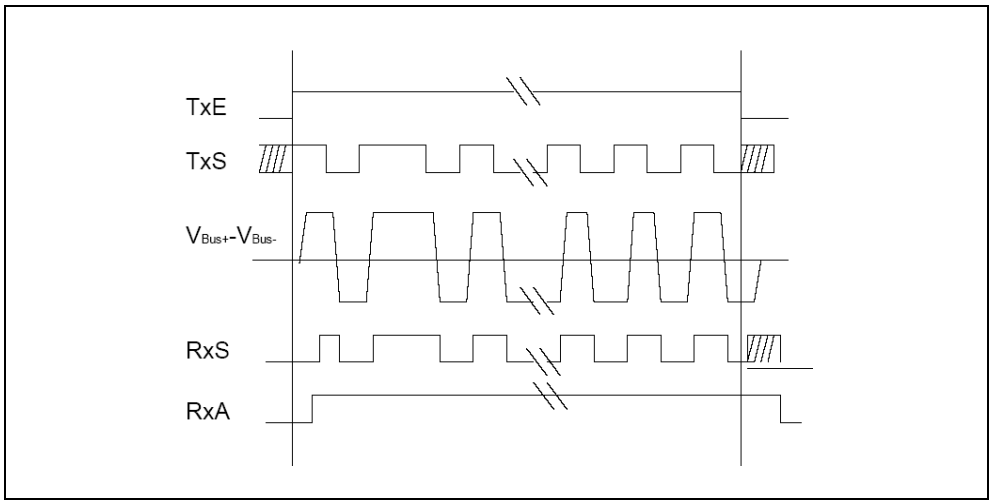


4.3 Signal Assignment

Description

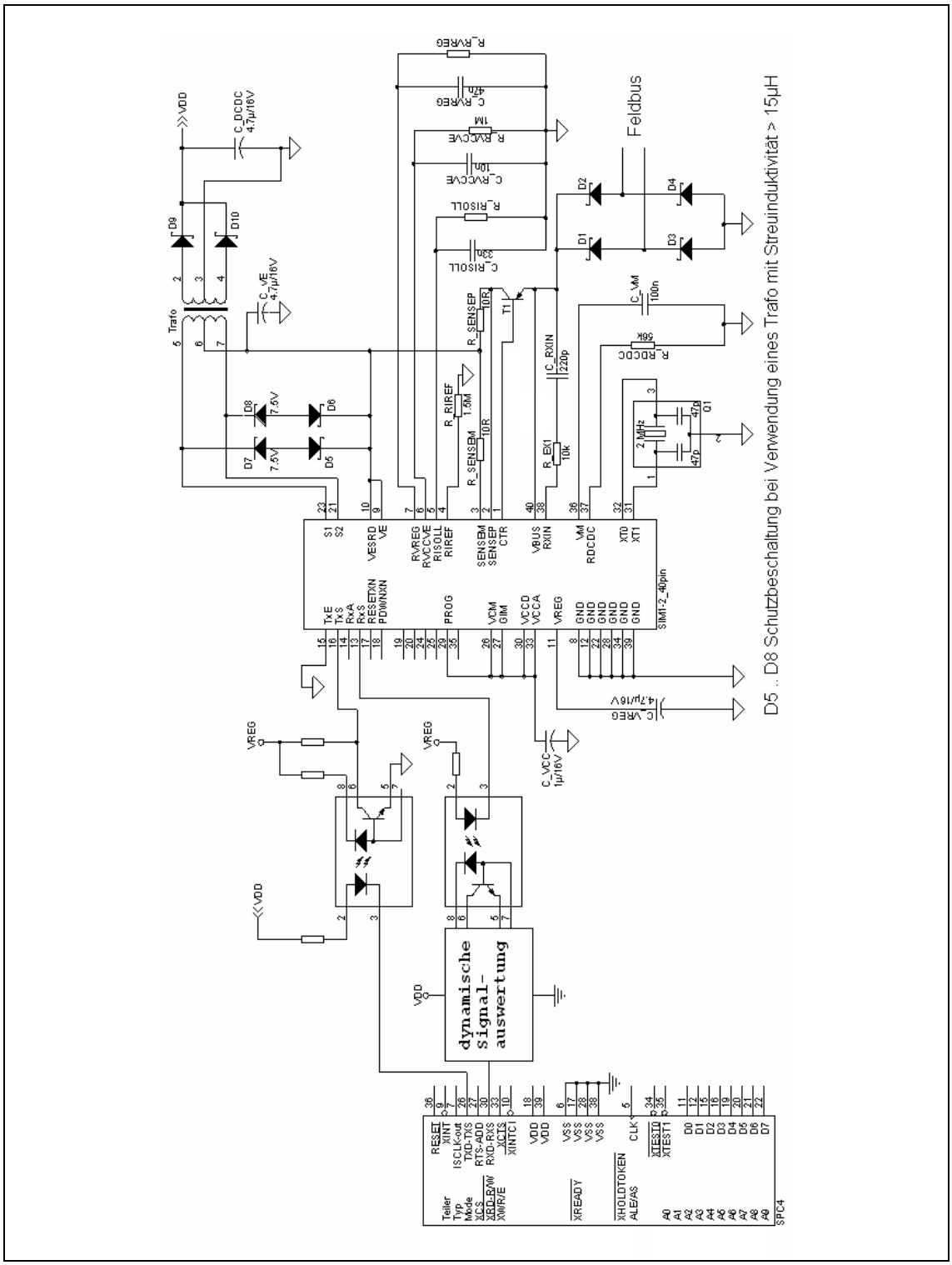
On the SIM 1-2, the signals are assigned in compliance with the IEC 61158-2 standard. The figure below describes the assignment of the logical state of TxS to the signal adjustment VBus+—VBus- (or the assignment of VBus+—VBus- to RxS).

Signal Assignment

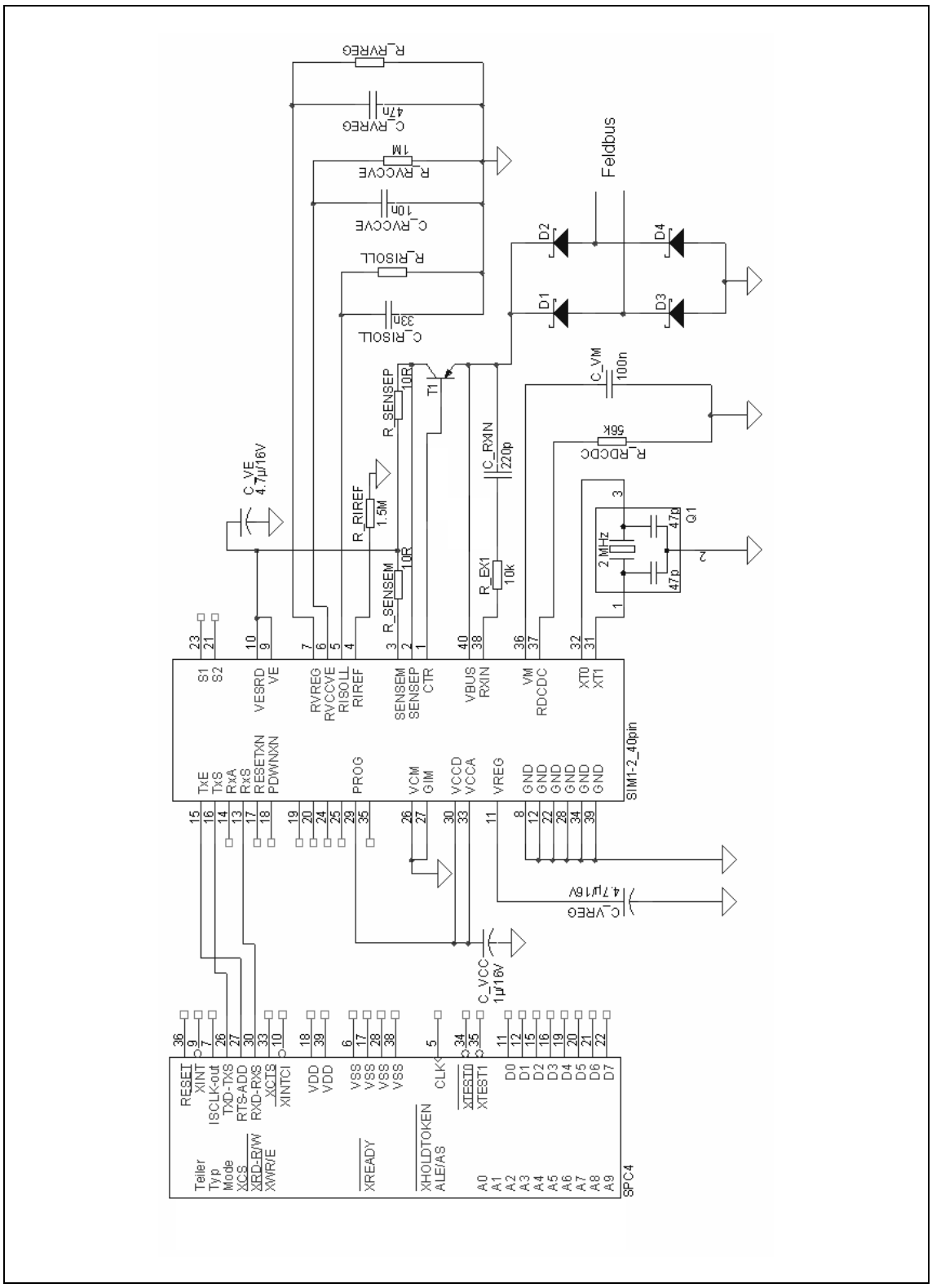


4.4 Circuit Examples

4.4.1 Block Diagram of the SIM 1-2 and SPC 4-2 with Galvanic Isolation



4.4.2 Diagram of the SIM 1-2 and SPC 4-2 without Galvanic Isolation



4.4.3 External Components (recommended values)

If you want to achieve the described accuracy of the SIM 1-2, the SIM 1-2 must be connected to the external components listed in the following table.

Name	Meaning	Type	Rated value	Unit	Tolerance	Temp. coeff.	Voltage
R_{SENSEM}, R_{SENSEP}	Actual current value detection	Metal layer	10	Ω	±0.1 %	15 ppm/K	
R_{RIREF}	Reference current generation	Metal layer	1.5	MΩ	±0.1 %	15 ppm/K	
R_{RISOLL}	Bus current setting	Metal layer	- 0.1 to 2.5	MΩ	±0.1 %	15 ppm/K	
R_{RVCCVE}	Reference voltage VCC, VE	Metal layer	1.0	MΩ	±0.1 %	15 ppm/K	
R_{VREG}	Reference voltage VREG	Metal layer	1.0 to 2.5	MΩ	±0.1 %	15 ppm/K	
R_{EX1}	Input high pass		10	kΩ	±1 %	100 ppm/K	
R_{RDCDC}	DC/DC startup current limitation		56	kΩ	±0.1 %	15 ppm/K	
C_{VE}	Backup capacitance	Tantalum TAJA475K016R, TAJC107K010R	4.7 to 100 *)	µF	±10 %		10 V
C_{VREG}	Backup capacitance	Tantalum TAJA475K016R, TAJA226K016R	4.7 to 22	µF	±10 %		10 V
C_{VCC}	Backup capacitance	Tantalum TAJA105K016R, TAJA335K016R	1.0 to 3.3	µF	±10 %		10 V
C_{VM}	Backup capacitance	Ceramic	100	nF	±5 %		
C_{RXIN}	Input high pass	Ceramic	220	pF	±5 %		
C_{RISOLL}	Backup capacitance	Ceramic	33	nF	±5 %		
C_{RVCCVE}	Backup capacitance	Ceramic	10	nF	±5 %		
C_{RVREG}	Backup capacitance	Ceramic	47	nF	±5 %		
C_{DCDC}	Backup capacitance	Tantalum	≤ 22	µF	±10 %		
D1-D4		Schottky	BAT86				
D5, D6		Schottky	BAT65				
D7, D8		Z-diode	BZX84C7 V5				
D9, D10		Schottky	BAT65				
t1	Transistor	PNP	PZT3906				
Q1	Murata CSTCC_G_A		2	MHz			
Transformer	Transformer						

*) At C_{VE} > 33 µF, it is recommended that a 1 Ω resistor is connected in series with C_{VE}

4.4.4 Notes on the Transistor

As an alternative to the recommended transistor PZT3906, the transistor PZT2907A can be used for I_{BUS} currents ≥ 10 mA. However to increase system stability (avoiding self excitation) an inductor (3.3 µH) must be included in series in addition to the RSENSEP measuring resistor (see section 2.3.3, "Current Sensing by SENSEP and SENSEM“).

Please not the following restrictions regarding EMC capacitance for the transistor PZT2907A:

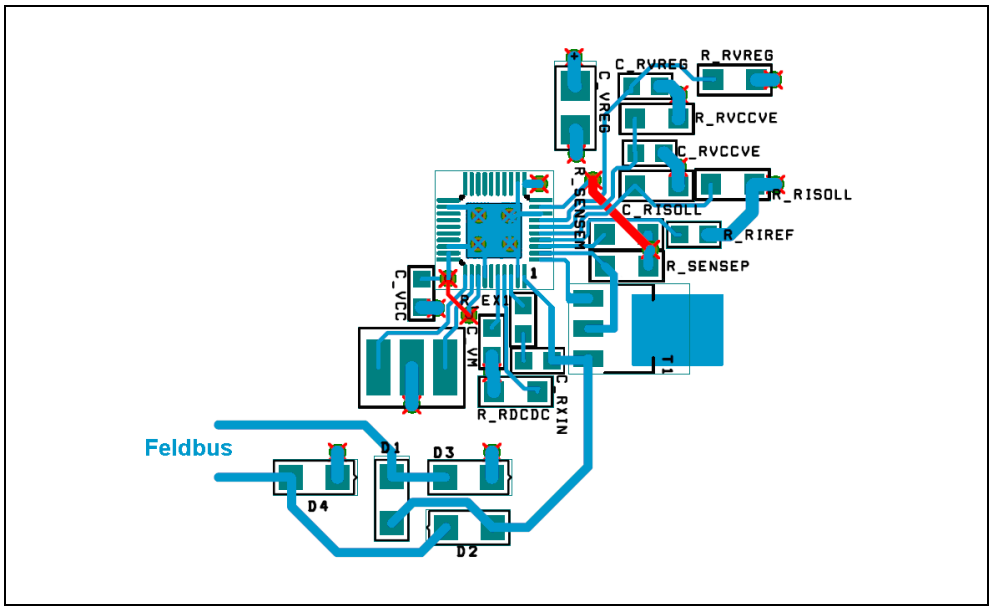
10 mA ≤ I_{BUS} ≤ 50 mA, C_{EMC} ≤ 500 pF

With the transistor PZT2907A and an EMC capacitance C_{EMC} ≤ 500 pF, the required impedance is achieved (at 39 kHz) for bus voltages U_{BUS} ≥ 9 V and 10 mA ≤ I_{BUS} ≤ 50 mA.

4.5 Layout Proposal

To ensure optimum functionality of the SIM 1-2, certain layout rules should be adhered to.

- Connection from pin CRT to base of T1 as short as possible
- Connection from SENSEP over RSENSEP to capacitor CVE and connection from SENSEM over RSENSEM to capacitor CVE as short as possible and symmetrical
- When using a transformer as DC/DC converter, this should be wired as short as possible to the switches S1 and S2 and the power supply VE.



Putting into Operation

5

5.1 Putting into Operation for the First Time

Description

Before putting into operation for the first time, check the correct wiring and components according to the block diagrams. In particular, check the reference resistances R_{RIREF}, R_{RISOLL}, R_{RVCCVE} and R_{RVREG} and the connection VE/VESRD and the connection VCCA/VCCD.

Caution

An interruption at the reference resistances R_{RIREF} and R_{RISOLL} during operation can lead to damage/destruction of the SIM 1-2.

5.2 Test Points

Description

To check the functionality, the following measurements can be made during operation.

Measured value	Description
VE	Voltage at pin VE/VESRD = 6.3 V
VCC	Voltage at pin VCCA/VCCD = 5.0 V
VREG	Voltage at VREG pin according to R_{RVREG} tolerance
IBUS	Total current consumption according to R_{RISOLL} tolerance

Check whether or not the voltages and the current are within the tolerance range resulting from the tolerance of the selected resistors from the tolerance calculation in section 2.3.7.

Appendix A

6.1 References

/1/ IEC 61158-2 Digital data communications for measurement and control – Fieldbus for use in industrial control systems, Part 2: Physical layer specification and service definition

/2/ PROFIBUS Test Guidelines for Field Devices according to "PROFIBUS-PA Profile for Process Control Devices, Version 3.0“, Version 3.1, April 2000, Order number 2.061

/3/ FOUNDATION™ Specification 31.25 Kbps Physical Layer Conformance Test

6.2 Addresses

PROFIBUS User Organization

PNO
Geschäftsstelle
Hr. Dr. Wenzel
Haid- und Neu- Straße 7
76131 Karlsruhe, Germany
Tel.: +49 721 9658 590

Technical Information in Germany and Europe

Siemens AG
A&D SE RD73
Postfach 2355
90713 Fürth, Germany

Tel.: +49 911 750 2080
Fax: +49 911 750 2100
E-mail: comdec@siemens.com

Technical Information Outside Europe

PROFIBUS Interface Center
One Internet Plaza
PO Box 4991
Johnson City, TN 37602 4991

Fax: +01 423 262 2103
BBS: +01 423 262 2576
E-mail: profibus.center@sea.siemens.com

❑