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ET 200X BM 147 CPU Basic Module

Manual

The following supplement is part of this documentation:

No.	Designation	Drawing number	Edition
1	Product information	A5E00385826-02	11/2005

This manual is part of the documentation package with the order number
6ES7198-8FA01-8BA0

Edition 05/2003
EWA-4NEB780602202-04

Safety Guidelines

This manual contains notices intended to ensure personal safety, as well as to protect the products and connected equipment against damage. These notices are highlighted by the symbols shown below and graded according to severity by the following texts:

Danger

indicates that death, severe personal injury or substantial property damage will result if proper precautions are not taken.

Warning

indicates that death, severe personal injury or substantial property damage can result if proper precautions are not taken.

Caution

indicates that minor personal injury can result if proper precautions are not taken.

Caution

indicates that property damage can result if proper precautions are not taken.

Notice

draws your attention to particularly important information on the product, handling the product, or to a particular part of the documentation.

Qualified Personnel

Only **qualified personnel** should be allowed to install and work on this equipment. Qualified persons are defined as persons who are authorized to commission, to ground and to tag circuits, equipment, and systems in accordance with established safety practices and standards.

Correct Usage

Note the following:

Warning

This device and its components may only be used for the applications described in the catalog or the technical description, and only in connection with devices or components from other manufacturers which have been approved or recommended by Siemens.

This product can only function correctly and safely if it is transported, stored, set up, and installed correctly, and operated and maintained as recommended.

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Siemens AG
Bereich Automation and Drives
Geschaeftsgebiet Industrial Automation Systems
Postfach 4848, D- 90327 Nuernberg

Preface

Purpose of the manual

This manual complements the *ET 200X Distributed I/O Device* manual. It describes all the functions of the BM 147 CPU basic module. It does not deal with functions that have general applicability to the ET 200X. You will find these in the *ET 200X Distributed I/O Device* manual (see also the Section “Integration in the information landscape”).

The information contained in this manual and in the *ET 200X Distributed I/O System* manual will enable you to operate the ET 200X with the BM 147 CPU basic module as a DP slave on the PROFIBUS-DP or in an MPI network. The master functionality of basic module BM 147-2 CPU is also described.

Required level of knowledge

Knowledge of the field of automation engineering is required to understand the manual.

Knowledge on how to use computers or other PC equipment (e.g. programming devices) under the Windows 95/98/2000 and NT operating system is also required. You should also be familiar with the STEP 7 basic software. Refer to the ”Programming with STEP 7 V5.x” manual.

Scope of validity of the manual

This manual is valid for basic module BM 147-1 CPU with the order number 6ES7 147-1AA10-0XB0 and for basic module BM 147-2 CPU with the order number 6ES7 147-2AA00-0XB0, as well as for the components of the ET 200X distributed I/O device specified in the *ET 200X Distributed I/O Device* manual.

Agreement: When features and functions of the basic modules are described in this handbook that apply to both modules, the designation BM 147 CPU will be used. The full designation is only used when a feature is described that only applies to one of the basic modules.

This manual contains a description of the components that were valid at the time the manual was published. We reserve the right to enclose a Product Information bulletin containing up-to-date information about new components and new versions of components.

Changes compared to the previous version

This manual contains the following changes that were made to the previous version of this manual, *Basic Module BM 147 CPU*, Edition 03:

- Module name changed to BM 147 CPU
- New order numbers for BM 147 CPU:
  - 6ES7 147-1AA10-0XB0 for BM 147-1 CPU
  - 6ES7 147-2AA00-0XB0 for BM 147-2 CPU
- Connections using ECOFAST technology
- No mechanical adjustment of the PROFIBUS address on the device
- Coexistent MPI/DP interface
- Additional DP master interface for BM 147-2 CPU
- New memory concept
- Additional communication utilities
- New blocks
- Micro Memory Card (MMC) up to 8 Mbytes
- Data archiving and project storage on MMC
- 32-bit run-time meter

The Instruction list is no longer integrated in the manual. Available commands with the runtimes and the execution times of the SFCs and SFBs can be found in the documentation package in the *operations list, S7-300, CPU 31xC, CPU 31x, IM 151-7 CPU, BM 147-1 CPU, BM 147-2 CPU*.

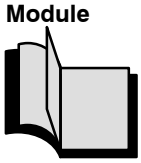
Standards, certificates and approvals

The BM 147 CPU basic module is based on the IEC 61784-1:2002 Ed1 CP 3/1 standard. It fulfills the requirements and criteria of IEC 61131, Part 2 and the requirements for obtaining the CE marking. For BM 147 CPU, the certifications for cULus have been applied for. You will find detailed information on these standards, certificates and approvals in the *ET 200X Distributed I/O Device* manual.

Position in the information landscape

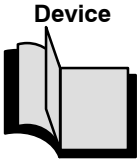
This manual is a component of the documentation package with the order number 6ES7 198-8FA01-8BA0. The package consists of 5 manuals with the following content:

BM 147 CPU Basic Module



- Addressing
- The ET 200X with the BM 147 CPU in the PROFIBUS network
- The ET 200X with the BM 147 CPU in the MPI network
- Commissioning and diagnostics
- Functions of the BM 147 CPU
- Technical specifications

ET 200X Distributed I/O Device



- Installation and wiring
- Commissioning and diagnostics
- Technical specifications of digital and analog modules
- Order numbers for digital and analog modules

EM 300 Motor Starter

- Wiring
- Commissioning and diagnostics
- Technical specifications
- Order numbers

EM 148-FC Frequency Converter

- Wiring
- Commissioning and diagnostics
- Functions and technical data

Instruction list S7-300 CPU 31xC, CPU 31x, IM 151-7 CPU, BM 147-1 CPU, BM 147-2 CPU

- The instruction set lists and their execution times.
- A list of executable blocks (OBs/SFCs/SFBs) and their execution times

Guide

The manual offers the following useful features that will assist you in rapidly finding the information you are looking for:

- At the beginning of the manual you will find a comprehensive table of contents and lists of the figures and tables in the manual.
- The sections of the chapters in the manual contain subheadings that allow you to gain a quick overview of the contents of the section.
- Important technical terminology used in the manual is defined in the Glossary.
- At the end of the manual you will find a comprehensive index enabling rapid access to the information you are looking for.

Special note

In addition to the ET 200X manuals, you will also need the manual for the DP master used and the documentation for the configuration and programming software used (see the list in Appendix A of the *ET 200X Distributed I/O Device* manual).

Note

You will find a detailed list of the contents of the ET 200X manuals in Section 1.2 of this manual.

We recommend that you begin by reading this section so as to find out which parts of which manuals are most relevant to you in helping you to do what you want to do.

Recycling and disposal

The components of the BM 147 CPU contain very few harmful substances which means that the unit can be recycled.

Please consult a certified disposal company specializing in electronics waste to ensure that your old device is recycled and disposed of in an environment-friendly manner.

Additional support

Please contact your local Siemens representative if you have any queries about the products described in this manual.
`http://www.siemens.com/automation/partner`

Training center

We offer courses to introduce you to the ET 200 distributed I/O system and the SIMATIC S7 programmable controller. Please contact your local training center or the central training center in Nuremberg, D-90327 Germany.
Telephone: +49 (911) 895-3200
Internet: `http://www.sitrain.com`

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Technical support and authorization staff generally speak English and German.		

Service & Support on the Internet

In addition to our documentation, we also offer you all of our know-how online on the Internet.

`http://www.siemens.com/automation/service&support`

There you will find:

- the newsletter, which constantly supplies you with the latest information on your products
- a search function in Service & Support to help you find the documents you need
- a forum in which users and specialists can exchange their experiences worldwide
- your local contact partner for Automation & Drives in our contact database
- information on on-site service, repairs and spare parts. You will find a lot more information under ”Services”.

Contents

Figures

Tables

Product Overview

1

In this chapter

The product overview provides information about

- The role of the BM 147 CPU basic module within the ET 200X distributed I/O device
- Which manuals in the ET 200X manual package contain what information.

In this chapter

1.1 What is the BM 147 CPU basic module?

What is the BM 147 CPU basic module?

The BM 147 CPU is a component of the ET 200X distributed I/0 device designed in the degrees of protection IP 65, IP 66 and IP 67. Unlike all other basic modules, the BM 147 CPU features integrated PLC functionality for pre-processing purposes. It enables you to decentralize control tasks.

An ET 200X with a BM 147 CPU can therefore exercise full and, if necessary, independent control over a process-related functional unit and can be used as a stand-alone CPU. The use of the BM 147 CPU leads to further modularization and standardization of technological functional units and simple, clear machine concepts.

How is the BM 147 CPU integrated in the ET 200X?

The BM 147 CPU basic module is integrated in the ET 200X in the same way as any other basic module. In other words, its configuration concept, installation and expansion capability are the same.

View

The figure below shows a sample configuration of an ET 200X with a BM 147 CPU.

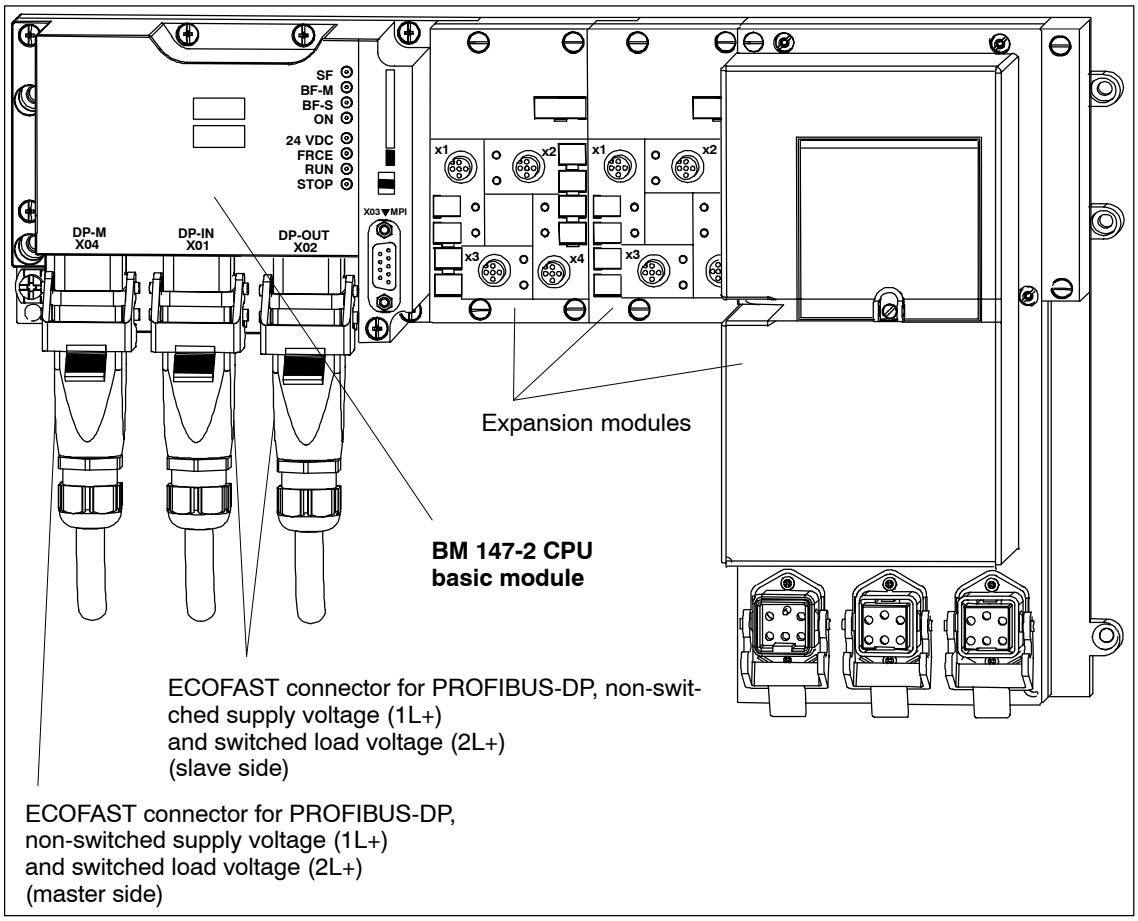


Figure 1-1 View of the ET 200X distributed I/O device with the BM 147 CPU

Interface

The BM 147 CPU has the following interfaces:

Table 1-1 Interface concept of the BM 147 CPU

Description	Functionality	Plug-in connection	Remarks on functionality
X01 (DP-IN)	MPI/DP slave interface (feed)	ECOFAST	Coexistent MPI/DP interface **one** logical interface
X02 (DP-OUT)	MPI/DP slave interface (looped through)	ECOFAST	
X03 (MPI)	MPI/DP PD interface	9-pin Sub-D socket	
X04 [1]) (DP-M)	DP master interface	ECOFAST	Additional DP master interface

1) Only featured in BM 147-2 CPU

Features of the BM 147 CPU in contrast to other basic modules

The BM 147 CPU basic module has the following special features:

- The basic module has PLC functionality (integrated CPU component with 48 kByte working memory).
- The basic module can only be operated with fitted load memory (MMC).
- The basic module does not have integrated inputs and outputs, but, like any other basic module, up to 7 expansion modules can be added to it from the ET 200X range.
- The basic module has an operating mode switch with positions for RUN, STOP and MRES.
- There are 8 LEDs on the front of the interface module to indicate the following:
  - ET 200X faults (SF)
  - Bus faults (BF-S and BF-M) (BF-M only in BM 147-2 CPU),
  - Non-switched supply voltage for electronics/sensors (1L+) (ON),
  - Switched load voltage (2L+) (24 VDC),
  - Force requests (FRCE)
  - Operating mode of the BM 147 CPU (RUN and STOP)
- The BM 147-2 CPU basic module also contains an additional interface with DP master functionality.

How is the ET 200X configured with the BM 147 CPU?

To configure the ET 200X with the BM 147 CPU (configuration and parameterization), you will require the *STEP 7* configuration software as of version V 5.2 + Service Pack 1. How to configure the ET 200X with the BM 147 CPU is described in Section 6.1 of this manual.

How is the BM 147 CPU programmed?

To program the BM 147 CPU, you will require the *STEP 7* configuration software as of version V 5.2 + Service Pack 1. In the *Instruction list*, you will find the *STEP 7* instruction set for programming the BM 147 CPU.

1.2 Guide to the ET 200X manuals

Components and the manuals required for them

The components of the ET 200X are described in various manuals in the ET 200X package. The figure below shows possible ET 200X configurations and the manuals required for them.

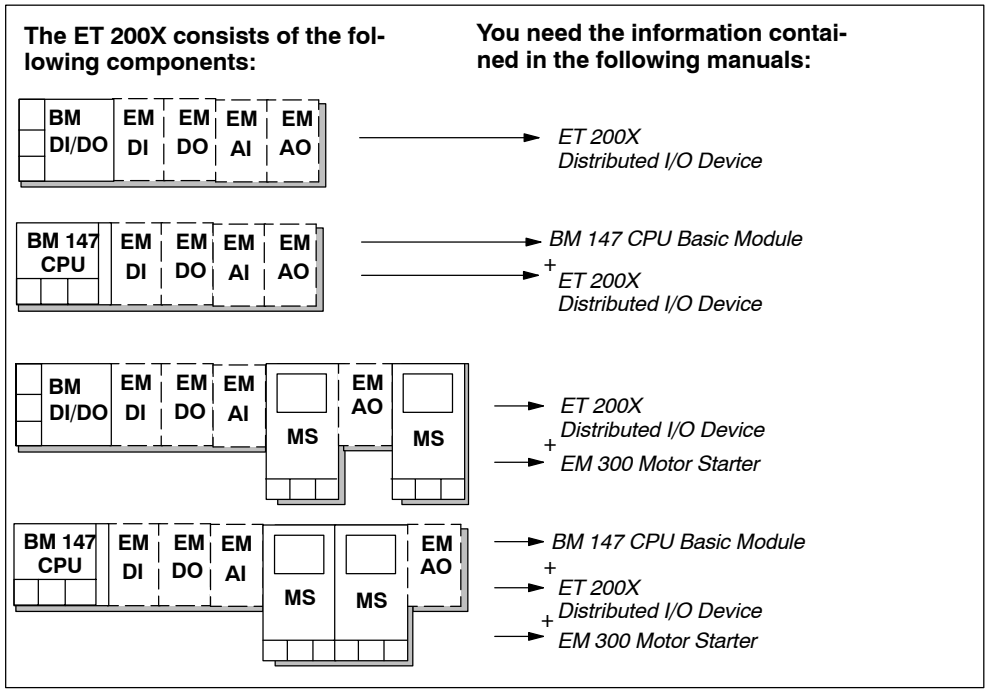


Figure 1-2 Components and the manuals required for them

Where do you find what information?

The table below will help you get your bearings and find the information you need quickly. It tells you which manual you need to refer to and which chapter deals with the topic you are interested in.

Table 1-2 Topics of the manuals in the ET 200X manual package

Contents	Manual			Chapter/ Appendix
	ET 200 X Distributed I/O Device	*BM 147 CPU Basic Module*	*EM 300 Motor Starter*	
ET 200X configuration options	x			2
Installing the ET 200X; setting the PROFIBUS address; connecting a terminating resistor	x			3
BM 147 CPU addressing		x		2
Electrical configuration and wiring of the ET 200X	x			4
Wiring motor starters			x	2
The ET 200X with the BM 147 CPU in the PROFIBUS network		x		3
The ET 200X with the BM 147 CPU in the MPI network		x		4
Mounting and wiring the BM 147 CPU		x		5
Commissioning and diagnostics of the ET 200X	x			5
Commissioning and diagnostics of the ET 200X with the BM 147 CPU		x		6
Commissioning and diagnostics of the ET 200X with motor starters			x	3
Functions of the BM 147 CPU		x		7
BM 147 CPU cycle and response times		x		8
General technical specifications of the ET 200X (standards, certificates and approvals, EMC, environmental conditions, etc.)	x			6
Technical specifications of the basic and expansion modules with DI, DO, AI and AO	x			7
Technical specifications of the BM 147 CPU		x		9
Technical specifications of the motor starters			x	5
Compatibility		x		10
Order numbers of the components	x			Q
Order numbers for the motor starters			x	Q
GSD files	x			B
Dimensioned drawings of the basic modules and digital and analog expansion modules	x			C
Dimensioned drawings of motor starters			x	B

Table 1-2 Topics of the manuals in the ET 200X manual package

Contents	Manual			Chapter/ Appendix
	ET 200 X Distributed I/O Device	*BM 147 CPU Basic Module*	*EM 300 Motor Starter*	
Configuration assignment frame for motor starters			x	C
Position of the BM 147 CPU in the CPU range		x		11
Glossary	x	x		Glossary

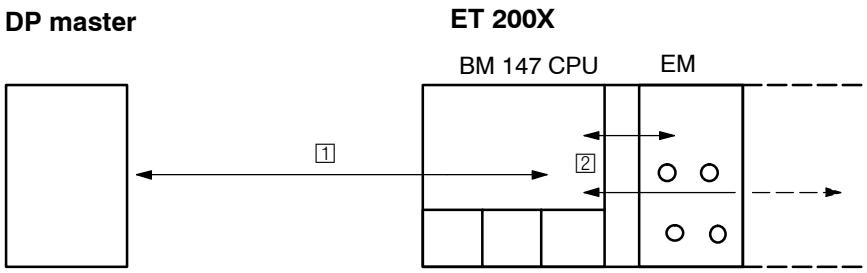
The frame for configuration and parameter assignment for the BM 147 CPU can be found on the Internet at `http://www.ad.siemens.de/simatic-cs`

Addressing

2

Principles of data interchange between the DP master and the ET 200X

The figure below illustrates both mechanisms of data interchange for which addresses are required in the ET 200X. In this chapter you will find all the information you need on the addressing of the ET 200X with the BM 147 CPU.



1 Data interchange between the DP master and the ET 200X via an intermediate memory in the BM 147 CPU

2 Data interchange between the BM 147 CPU and expansion modules

Figure 2-1 Principles of data interchange between the DP master and the ET 200X with the BM 147 CPU

In this chapter

2.1 Slot-based addressing

Slot-oriented address allocation

In slot-based addressing (default addressing), each of a module's slot numbers is assigned an address area in the BM 147 CPU.

Depending on the type of the expansion module, the addresses are digital or analog (see Table 2-1). The address allocation is not fixed and can be changed, but there is a default address area.

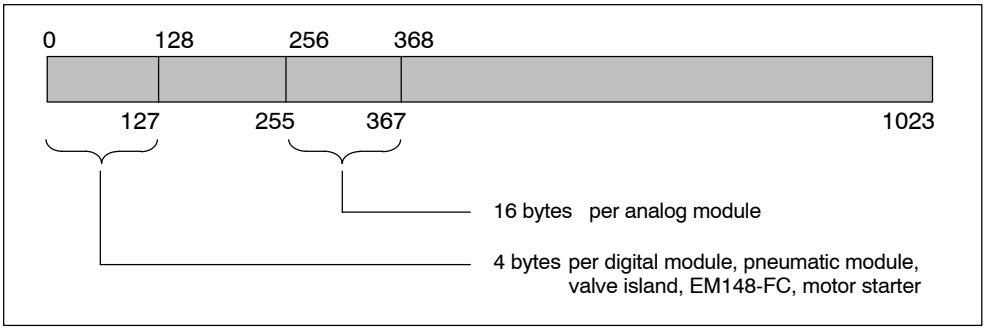


Figure 2-2 Structure of the default address area

Slot assignment

The figure below shows an ET 200X configuration with 7 expansion modules (maximum configuration) and the slot assignment.

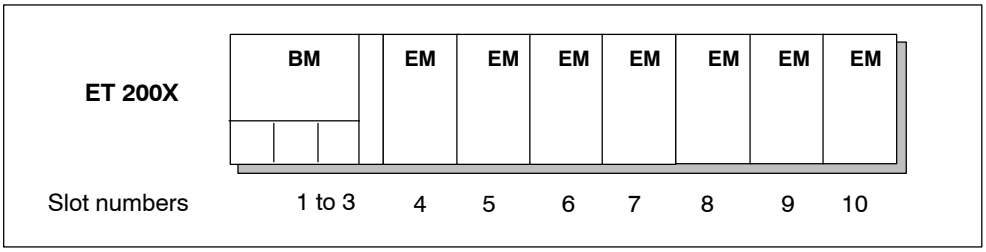


Figure 2-3 Slots on the ET 200X

Slot rules

When assembling an ET 200X with extension modules and pneumatic interface modules, follow the rules in the *ET 200X Distributed I/O Device manual,* Chap. 2.8.

Address assignment

For each of the expansion modules, of which there can be up to seven, 4 bytes are reserved for digital I/O devices and 16 bytes for analog I/O devices, depending on the slot, in the address areas of the BM 147 CPU.

The table below indicates the fixed address assignment for analog and digital modules per slot. The address areas of the expansion modules are ”visible” only to a BM 147 CPU in the ET 200X, not to the associated DP master. The DP master has no access to the expansion modules.

Table 2-1 Addresses of the ET 200X expansion modules

Reserved address area	Slot number									
	1	2	3	4	5	6	7	8	9	10
Digital modules	Basic module			0 to 3	4 to 7	8 to 11	12 to 15	16 to 19	20 to 23	24 to 27
Analog modules				256 to 271	272 to 287	288 to 303	304 to 319	320 to 335	336 to 351	352 to 367

The unassigned addresses in the range 28 to 127 are in the process image in default addressing and can be used any way you choose in the user program. If 4 bits in a byte are already used, the remaining 4 bits cannot be used.

You can use the bytes in the address areas that are not used by modules in any way you choose in your user program. In the configuration in Figure 2-4, for example, bytes 1, 2 and 3 can be used as you choose.

Example of address assignment to expansion modules

The figure below illustrates a sample ET 200X configuration, showing address allocation for expansion modules by way of example. The addresses for the expansion modules are predefined in default addressing.

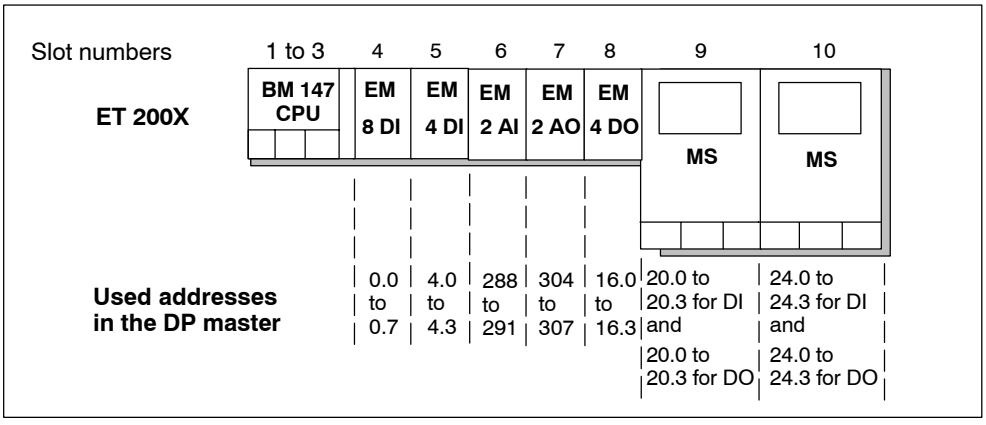


Figure 2-4 Example of address assignment to expansion modules

2.2 User-oriented addressing of the expansion modules

User-oriented address allocation

User-oriented address allocation means you can select the following in units of 1 byte and independent of one another within the range 0 to 1023:

- Input addresses of expansion modules and
- Output addresses of expansion modules.

The addresses 0 to 127 are in the process image. Assign the addresses in *STEP 7*. When you do this, you define the base address of the module, on which all the addresses of the module depend.

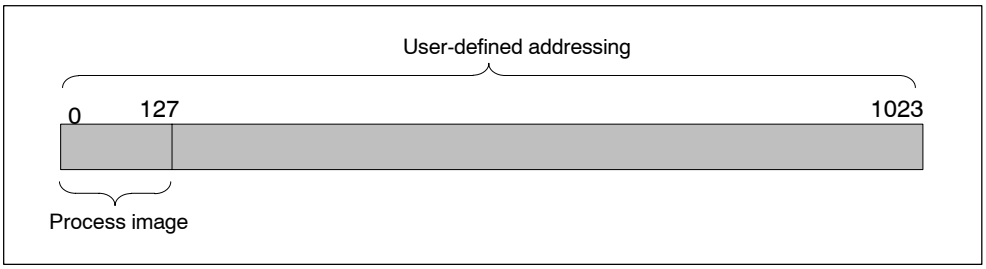


Figure 2-5 Structure of the address area for user-oriented addressing

Advantages

Advantages of user-defined address allocation:

- Optimum utilization of the address areas available, since ”address gaps” between the modules do not occur.
- When creating standard software, you can specify addresses that are independent of the configuration of the ET 200X station.

2.3 Data interchange with the DP master

User data transfer via an intermediate memory

The user data is located in an intermediate memory in the BM 147 CPU. This intermediate memory is always used when user data is transferred between the BM 147 CPU and the DP master. The intermediate memory consists of a maximum of 32 address areas.

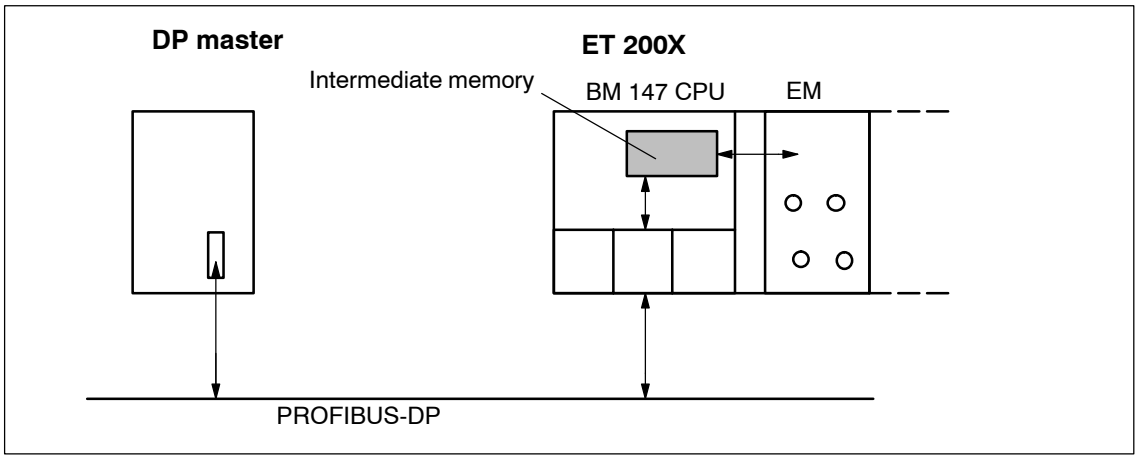


Figure 2-6 Intermediate memory in the BM 147 CPU

Address areas for user data transfer with the DP master

The ET 200X provides the PROFIBUS-DP with a maximum of 244 bytes of input data and 244 bytes of output data. This data can be addressed in the intermediate memory of the BM 147 CPU in up to 32 address areas.

An address area contains a maximum of 32 bytes. A maximum of 244 bytes is available for input and output data.

Data consistency

You define data consistency as byte, word, or overall consistency per address area. Consistency can amount to up to 32 bytes/16 words per address area.

DP diagnostic address in *STEP 7*

When the ET 200X is configured with *STEP 7*, two diagnostic addresses are set. The ET 200X receives information on the status of the DP master or on a bus interruption by means of these diagnostic addresses (see Section 6.5). In DP slave mode, the diagnostic addresses are by default at:

BM 147-1 CPU	BM 147-2 CPU	
1021	1020	Address for slot 2
1022	1021	Slave diagnosis address

Detailed information can be found in the *Online Help for STEP 7* under *Slot model for I slaves*.

Access to free areas in the process image

If you access available but unconfigured process image areas, no process image errors will be generated. You can therefore use inputs and outputs in the process image to which no I/O modules are allocated as markers.

2.4 Accessing the intermediate memory in the BM 147 CPU

Access in the user program

The following table tells you how to access the intermediate memory in the BM 147 CPU from the user program.

Table 2-2 Accessing the address areas

Access dependent on data consistency	The following applies
1, 2 or 4-byte data consistency with load/transfer instructions	All areas parameterized with ”unity” consistency can be accessed. A maximum of 32 bytes of input data can be addressed with load instructions and 32 bytes of output data with transfer instructions (L PEB/PEW/PED; T PAB/PAW/PAD; see also *Instruction list*). The data consistency for word addressing is 2 bytes; for double-word addressing it is 4 bytes. Access is also possible via the process image.
1- to 32-byte data consistency on the PROFIBUS-DP with SFC 14 and SFC 15	If the address area of consistent data is in the process image, this area is updated automatically. If you want to access data in the intermediate memory, you have to read the input data with SFC 14 ”DPRD_DAT” and write the output data with SFC 15 ”DPWR_DAT”. These SFCs have data consistency of 1 to 32 bytes. You can only copy the input data read with SFC 14 as a block of 1 to 32 bytes to a memory marker address area, for example, where it can be addressed with A M x.y. You can also write only one block of 1 to 32 bytes as output data with SFC 15 (see also the *System and Standard Functions*) Reference Manual. If you access areas with ”whole length” consistency, the length in the SFC must correspond to the length of the parameterized area. It is also possible to address the consistent areas directly (for example, L PIW or T PQW).

Rules for address allocation

You must obey the following rules when allocating addresses for the ET 200X with the BM 147 CPU:

- Assignment of the address areas:
  - Input data for the ET 200X is **always** output data for the DP master
  - Output data for the ET 200X is **always** input data for the DP master
- You access the data in the user program using load/transfer instructions or SFCs 14 and 15.
- The length, unit and consistency of the associated address areas for the DP master and the DP slave must be identical.
- Addresses for the master and the slave can be different in the logically identical intermediate memory (mutually independent logical I/O address areas in the master and the slave CPU)

When the BM 147 CPU is configured with *STEP 7* for operation in the S5 or in non-Siemens systems, it is clear that only the logical addresses within the slave CPU are allocated. The addresses are then assigned in the master system using the specific configuration tool of the master system.

Addressing interface in *STEP 7*

The following table illustrates the principles of address allocation. You will also find this table in the *STEP 7* interface. You must set the mode ”MS” (for master slave) or ”DX” (direct connection) in *STEP 7* (see Section 3.5).

Table 2-3 Addressing interface in *STEP 7 (extract)*

	Mode	**Master**		**PROFIBUS-DP partner**		**Parameters**		
		I/O	Address	I/O	Address	Length	Unit	Consistency
1	MS	Q	200	I	128	4	Byte	Unit
2	MS	Q	300	I	132	8	Byte	Total length
3	MS	I	700	Q	128	4	Word	Unit
4	MS	I	50	Q	136	4	Byte	Unit
:								
7								
	MS: Master Slave	Address areas in the DP master CPU		Address areas in the BM 147 CPU		These address area parameters must be identical for the DP master and the BM 147 CPU		

Sample Program

Below you will see a sample program for data interchange between the DP master and the DP slave.

You will find the addresses in Table 2-3.

SFCs 14 and 15 are called by specifying the logical address in hexadecimal format.

in the BM 147 CPU

```
Data preprocessing in the DP slave:

L       2                           Load actual value 2 and
T       MB      6                   transfer to memory byte 6.
L       IB      0                   Load input byte 0 and
T       MB      7                   transfer to memory byte 7.
```

```
Forward data to DP master

L       MW      6                   Load memory word 6 and
T       PQW     136                 transfer to peripheral output word 136
```

in the DP Master CPU

```
Postprocess received data in the DP master:

L       PIB     50                  Load peripheral input byte 50 and
T       MB      60                  transfer to memory byte 60.
L       PIB     51                  Load peripheral input byte 51 and
L       B#16#3                      load byte 3;
+       I                           add the values as integer data type and
T       MB      61                  transfer the result to memory byte 61.
```

```
Data preprocessing in the DP master:

L       10                          Load actual value 10 and
+       3                           add 3,
T       MB      67                  transfer the result to memory byte 67.
```

```
Send the data (memory bytes 60 to 67) to the DP slave:

CALL    SFC     15                  Call system function 15:
 LADDR:= W#16#12C                   Write the data to the output address area as of
 RECORD:= P#M60.0 Byte8             address 300 (12C hexadecimal) with a length of 8
 RET_VAL:=MW 22                     bytes as of memory byte 60.
```

in the BM 147 CPU

```
Receive data from the DP master (stored in MB 30 to 37):

CALL    SFC     14                  Call system function 14:
 LADDR:= W#16#84                    Write the data from the input address area as of
 RET_VAL:=MW 20                     address 132 (84 hexadecimal) with a length of 8
 RECORD:=P#M30.0 Byte8              bytes to memory byte 30.
```

```
Postprocess received data:

L       MB      30                  Load memory byte 30 and
L       MB      37                  load memory byte 37;
+       I                           add the values as integer data type and
T       MW      100                 transfer the result to memory byte 100.
```

User data transfer in STOP mode

The user data in the intermediate memory is processed differently depending on whether the DP master or the DP slave (BM 147 CPU) goes into STOP mode.

- The BM 147 CPU goes into STOP mode: The data in the intermediate memory (outputs only from the slave's viewpoint) of the BM 147 CPU are overwritten with ”0”; i.e. the DP master or a recipient in direct communication reads ”0”.
- If the DP master goes into STOP mode: The current data in the intermediate memory of the BM 147 CPU (inputs in the slave, outputs in the master) are retained and can be read out in the user program of the BM 147 CPU.

IM 308-C as the DP master (SIMATIC S5)

If you use an IM 308-C as the DP master, the following applies to the interchange of consistent data:

You must program FB 192 in the IM 308-C to enable the transfer of consistent data between the DP master and the DP slave. The effect of FB 192 is that the data is only output or read out by the ET 200X continuously in a single block.

ET 200X in the PROFIBUS Network

3

Introduction

You can integrate the ET 200X with the BM 147 CPU as a node in a PROFIBUS network. This chapter contains a description of a typical network configuration with the BM 147 CPU. It also tells you which functions can be executed via the PD or OP on the ET 200X and which options are available for direct connection. The available communication utilities can be found in Section 7.8.

Equidistance

As of *STEP 7* V 5.2 + SP1, you can parameterize bus cycles of the same length (equidistant) for PROFIBUS subnets with BM 147 CPU. You will find a detailed description of the functions in the *Online Help for STEP 7*.

In this chapter

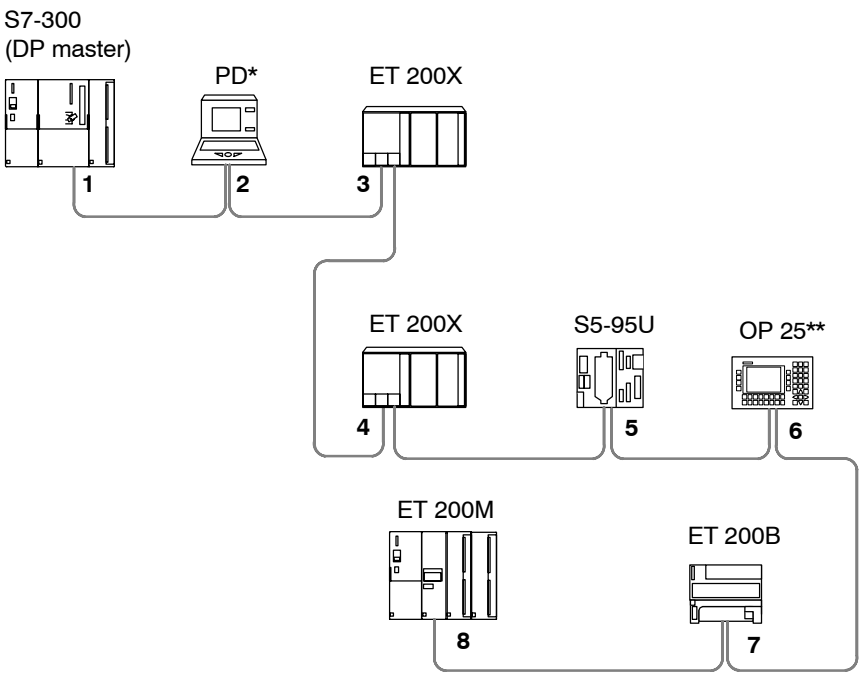
More information

You will find more information on the structure of networks in the manual for the DP master.

3.1 ET 200X in the PROFIBUS network

Structure of a PROFIBUS network

The figure below illustrates the basic structure of a PROFIBUS network with one DP master and several DP slaves.



*** The ET 200X can be configured and programmed from this programming device**
**** Operating and monitoring functions can be executed on the ET 200X**
1 ... 8 PROFIBUS addresses of the nodes

Figure 3-1 Example of a PROFIBUS network

Hardware requirements in the programming device/OP for accessing the ET 200X

Before you can access a BM 147 CPU from a programming device/operator panel, the programming device/operator panel must fulfill the following requirements:

- it must have an integrated PROFIBUS-DP interface or DP card; or
- it must have an integrated MPI interface or MPI card.

Access to the ET 200X

The BM 147 CPU is a passive/active bus node. The programs and configuration of the BM 147 CPU can be transferred to the BM 147 CPU by choosing ”Load PLC” from the PD in SIMATIC Manager. All the other diagnostic and test functions are also possible with the PD.

If the PD is currently the only active bus node, this must be set beforehand in SIMATIC Manager by choosing the ”Set PD/PC Interface” menu command (see Section 3.4).

However, you can still install OPs/OSs (operator panels/operator stations) as fixed components of the PROFIBUS network for operating and monitoring functions.

You cannot access an ET 200X from more than 12 devices in parallel:

- 1 connection is reserved for the PD.
- 1 connection is reserved for an OP or an OS.
- 10 connections are available as desired for PDs, OPs/OSs and CPUs.

We recommend that you allocate a PROFIBUS address to the PD/OP in the same way as for other network nodes (see Figure 3-1).

Active/passive DP interface of the BM 147 CPU

You set the mode of the DP interface at the BM 147 CPU during configuration in the **Properties – MPI/DP** window:

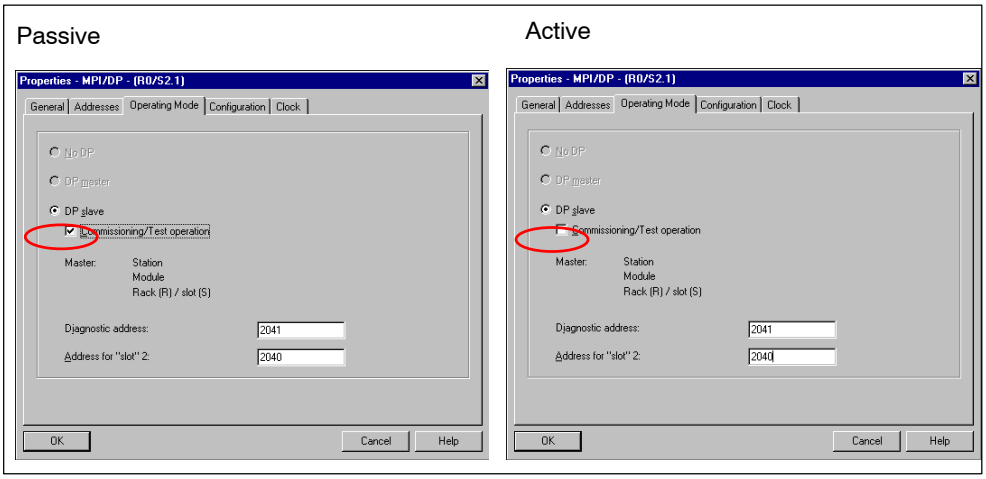


Figure 3-2 Setting the mode of the DP interface at the BM 147 CPU

Depending on the DP interface setting, the BM 147 CPU will behave in the following way:

Table 3-1 Behavior of the BM 147 CPU depending on the DP interface setting

	DP interface of the BM 147 CPU	
	Passive	**Active**
Transmission rate detection	Yes	No
Testing and commissioning functions	Slow	Fast
Bus cycle time	Fast	Slow
Diagnosis via BF LED	See Section 6.4	
Routing (only for BM 147-2 CPU)	No	Yes

Maximum data transfer rate and cable length with a PD connecting cable

You can obtain a maximum data transfer rate of 1.5 Mbaud using the PD connecting cable. The cable length may not exceed 3 meters.
The PD connecting cable should only be connected for an extended period of time during startup and service.

Data transfer rates over 1.5 MBaud require an active connecting cable for the PD connection (for order information, see Appendix A).

Note

A PD connecting cable on the X03 interface forms a spur line to the X01 and X02 interfaces. In this way, for example, an error for this DP segment can be output through use of a diagnosis repeater. Therefore, you should also use an active spur line for baud rates lower than or equal to 1.5 MBaud (for order information, see Appendix A).

Examples of PD/OP connection to ET 200X

- The PD/OP is connected to the PROFIBUS-DP interface of the DP master, but can be connected just as well to any other station in the DP network, including the ET 200X.

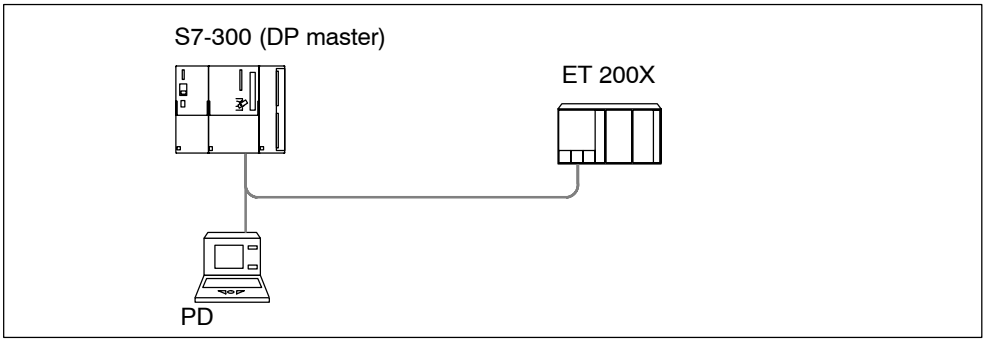


Figure 3-3 PD/OP accesses the ET 200X via the DP interface in the DP master

- The PD is directly connected to the ET 200X (you don't add the ET 200X to the PROFIBUS network until later).
  Note: Depending on the DP interface (active/passive), a special setting is required in *STEP 7* (see Section 3.4).

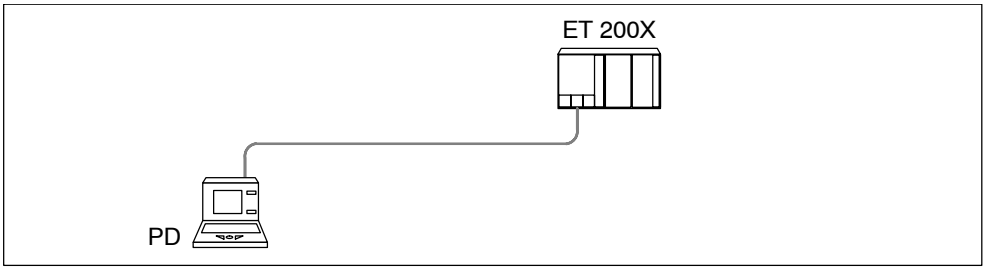


Figure 3-4 The PD directly accesses the ET 200X

- The PD can also be a direct DP node, although a spur line (e.g. PD connecting cable) is not permissible with a transmission rate greater than 1.5 Mbaud. This requires an active spur line.

3.2 Network components

To connect the ET 200X to the PROFIBUS-DP network, you will require the network components listed in the Appendix A.

Example of the use of network components

The figure below shows the example from Figure 3-3 with the use of the network components. Connecting the bus cable to the bus connector is described in the Product Information document for the bus connector.

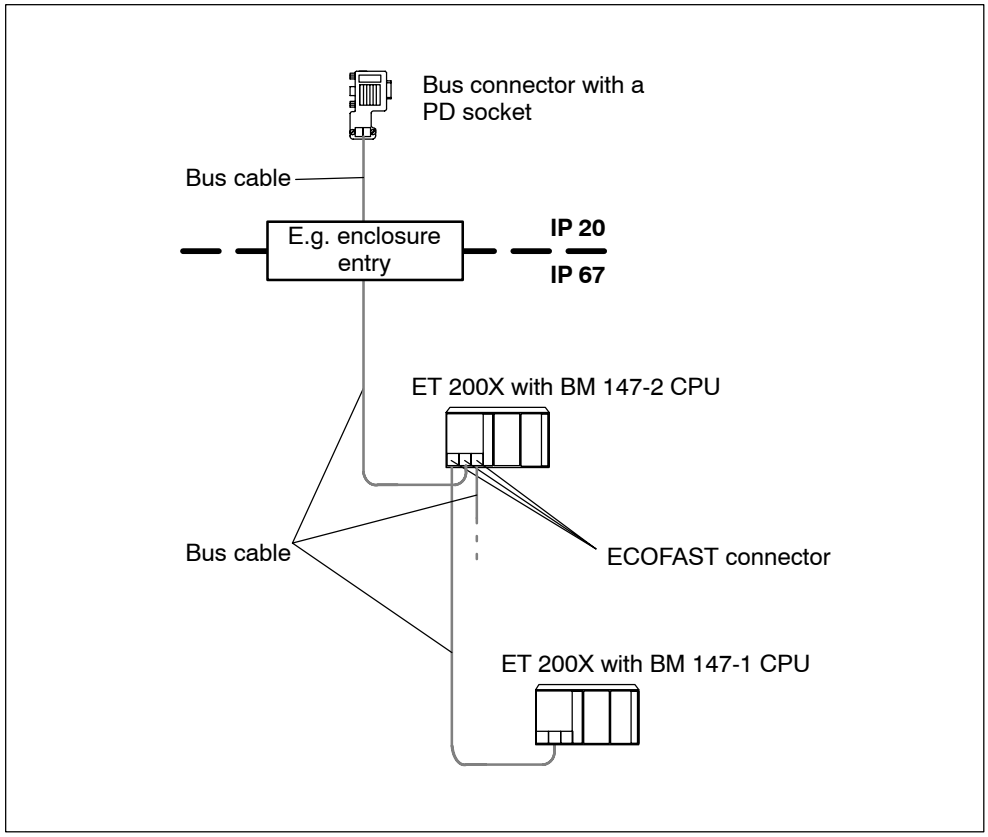


Figure 3-5 Connecting the DP network

3.3 PROFIBUS address

Features

Use the PROFIBUS address to specify the address at which the BM 147 CPU is contacted on the PROFIBUS-DP.

Prerequisites

- The permitted PROFIBUS-DP addresses are 1 to 125.
- Each address can be allocated only once on the PROFIBUS-DP.

Startup without DP configuration on the Micro Memory Card (MMC) (initial startup)

Following POWER ON, the coexistent interface on the BM 147 CPU powers up as an MPI interface with the address 2, HSA 31 and 187.5 kBaud. The DP slave functionality of the BM 147 CPU is not yet available. All PD functions listed in Section 3.4 are possible with the interface.

Several ET 200X units with BM 147 CPUs as DP slaves on one PROFIBUS network must be commissioned step by step. After each individual BM 147 CPU has been switched on, STEP 7 must be used to transfer a configuration with DP address to the BM 147 CPU.

Note

The bus parameters are retentive, i.e. bus parameters that have been configured (e.g. address, transmission rate) are retained

- with POWER OFF
- if there is no longer a configuration on the BM 147 CPU (e.g. after SDBs have been deleted or following POWER ON without MMC)

Startup with DP configuration on the Micro Memory Card (MMC)

As soon as a DP configuration has been downloaded to the BM 147 CPU, the data stored on the MMC is used on startup.

Following POWER ON, the BM 147 CPU as the DP slave powers up with the configured address and waits for parameter assignment by the DP master.

As active PROFIBUS node, the BM 147 CPU adopts the configured transmission rate.
As passive PROFIBUS node, the BM 147 CPU searches for the transmission rate.

3.4 Functions via the PD/OP

You can use the programming device to:

- Configure the BM 147 CPU with ET 200X modules and put them into operation on the PROFIBUS-DP
- Program the BM 147 CPU.
- Execute test functions such as ”Monitor/Modify Variables” and ”Program Status”

  Execute commissioning functions such as ”Start” and ”Memory Reset”
- Display the module status (i.e. for the BM 147 CPU, for example, you can display the utilization of the load and working memory, stack contents and diagnostic buffer contents)

You can use the OP to:

- Operate and monitor

You will find a detailed description of the functions in the online help for *STEP 7*.

Running the BM 147 CPU as a passive DP slave on the PD – required settings in *STEP 7*

If you connect a BM 147 CPU directly to a PD, you must set the PD interface in *STEP 7* to allow communication between the two partners. Proceed as follows:

1. In *STEP 7*, choose the “Setting the PD/PC Interface” tool (**Start > STEP 7 > Setting the PD/PC Interface**).
2. Set the interface of your PD to PROFIBUS.
3. Call the properties of the PROFIBUS network.
4. Set the properties so that the PD/PC is the only active master on the bus.

Later, after you have configured a DP master for the network and have gone online, you should reset these settings as this activates additional safety functions against bus faults.

Force test function

In the case of the BM 147 CPU, you can preset the inputs and the outputs in the process image with fixed values using the ”Force” function.

The values (force values) you have preset can still be controlled in the BM 147 CPU by the user program and by PD/OP functions. This is shown in Figure 3-6.

You can force a maximum of 10 variables with the BM 147 CPU.

Caution

The force values in the process-image input table can be overwritten by write commands (for example T IB x, = I x.y, copy with SFC, etc.) as well as by I/O read commands (L PIW x, for example) in the user program or by PD/OP write functions.

Outputs preset with force values only return the force value provided the user program does not execute any write accesses to the outputs using I/O write commands (e.g. T PQB x) and provided no PD/OP functions write to these outputs.

It is important to note that force values in the process-image input/output table cannot be overwritten by the user program or by PD/OP functions.

Principle behind forcing with the BM 147 CPU

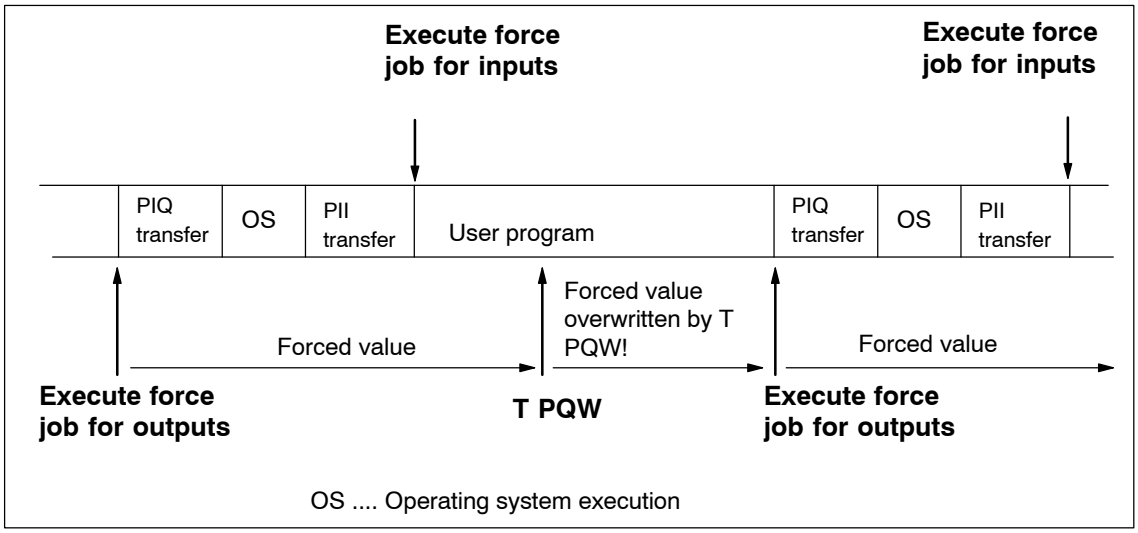


Figure 3-6 Principle behind forcing

Application example

Prerequisite: There is no direct I/O access in your user program.

If, for example, an enable sensor (f) in your system is defective and it continually indicates a logical 0 to your user program, for example, via input 1.2, you can bridge this sensor by forcing the input to 1, ensuring that your system continues to operate.

Warning

However, because the sensor is out of operation, you must monitor the functionality by different means to avoid injury to the operator and damage to the machine.

3.5 Direct communication

You can configure the BM 147 CPU as an intelligent slave as of *STEP 7* V5.2 for direct communication. Direct communication is a special communication relationship between PROFIBUS-DP nodes.

Principle

Direct communication is characterized by the fact that the PROFIBUS-DP nodes ”listen in” to find out which data a DP slave is sending back to its DP master. Using this function, the eavesdropper (recipient) can directly access changes to the input data of remote DP slaves.

During configuration in *STEP 7*, you set via the relevant I/O input addresses the address area of the recipient at which the required data of the sender is to be read.

Example

Figure 3-7 shows an example of the relationships you can configure in the *STEP 7* for the direct data exchange with a BM 147 CPU. Other DP slaves can only be senders here.

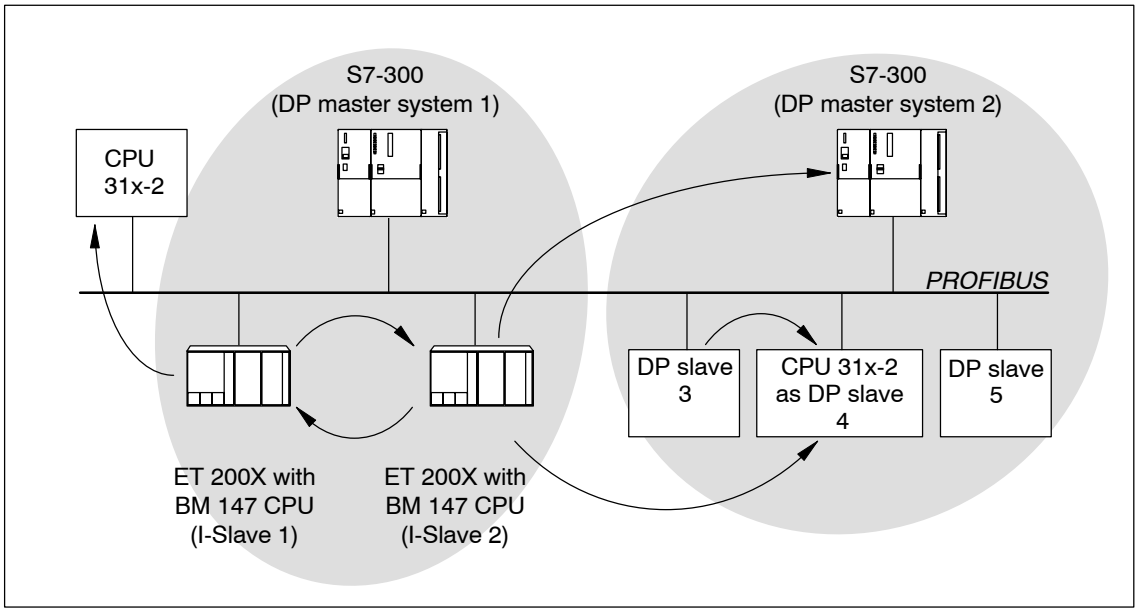


Figure 3-7 Direct communication with the BM 147 CPU

Functionality in direct communication

The BM 147 CPU offers the following functionality in direct communication:

- Transmitter:
  As a DP slave, the BM 147 CPU sends the process outputs, configured for direct communication, to all bus nodes as a broadcast frame. Other recipients filter the relevant data from this broadcast frame.
- Receiver:
  Filtering of the data from the broadcast frame sent by transmitters which have been configured using *STEP 7* as being relevant for direct communication.

Diagnostics in direct communication

Only the results of connection monitoring can be used in the diagnostics of the DP slaves configured for direct communication, because diagnostic messages of the DP slaves that have been listened in on are only reported to the DP master.

The asynchronous OB 86 is called in the event of station failure and reintegration. If data is accessed during a station failure of the sender, an I/O access error is detected and OB 122 is called. Only the identifiers ”module plugged” and ”module available” are relevant for the module status data.

ET 200X in the MPI Network

4

Introduction

You can integrate the ET 200X with the BM 147 CPU as a node in an MPI network. This chapter contains a description of a typical network configuration with the BM 147 CPU. Section 3.4 describes which functions can be executed on the BM 147 CPU using a PD or OP. The available communication utilities can be found in Section 7.8.

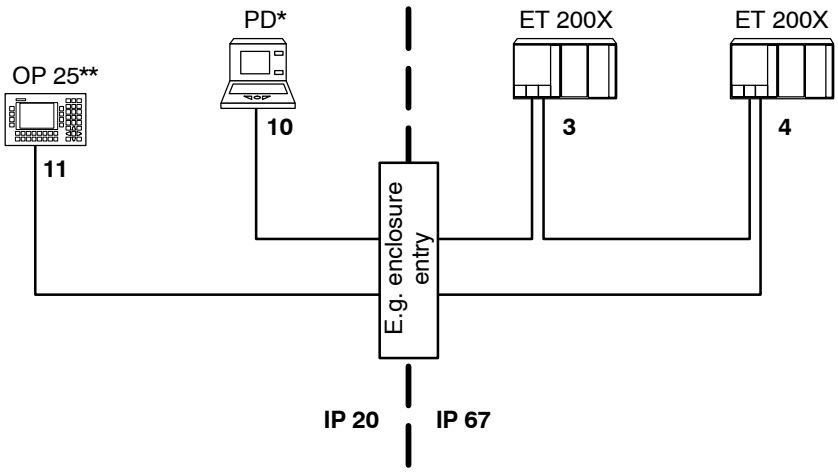
Information on clock synchronization via the MPI interface is found in the *STEP 7 Online Help*.

In this chapter

4.1 ET 200X in the MPI network

Structure of an MPI network

The figure below shows an example of an MPI network configuration.



***** **The ET 200X can be configured and programmed from this programming device**

****** **Operating and monitoring functions can be executed on the ET 200X**

3, 4, 10, 11 MPI addresses of the nodes

Figure 4-1 Example of an MPI network

Hardware requirements in the programming device/OP for accessing the ET 200X

Before you can access a BM 147 CPU from a programming device/operator panel, the programming device/operator panel must fulfill the following requirements:

- it must have an integrated MPI interface or MPI card or
- it must have an integrated PROFIBUS-DP interface or DP card.

Transmission rates

In the MPI network, all MPI transmission rates are possible with the BM 147 CPU.

Network components

You configure an MPI network using the same network components as those used for a PROFIBUS-DP network (see Section 3.2).

Maximum data transfer rate and cable length with a PD connecting cable

You can obtain a maximum data transfer rate of 1.5 Mbaud using the PD connecting cable. The cable length may not exceed 3 meters.
The PD connecting cable should only be connected for an extended period of time during startup and service.

Data transfer rates over 1.5 MBaud require an active connecting cable for the PD connection (for order information, see Appendix A).

Note

A PD connecting cable on the X03 interface forms a spur line to the X01 and X02 interfaces. In this way, for example, an error for this MPI segment can be output through use of a diagnosis repeater. Therefore, you should also use an active spur line for baud rates lower than or equal to 1.5 MBaud (for order information, see Appendix A).

4.2 MPI address

Features

With the MPI address, you determine the address under which the BM 147 CPU is accessed in the MPI network.

Prerequisites

- The permitted MPI addresses are 0 to 126.
- Each address can be allocated only once on the MPI network.

Recommendations for MPI addresses

- Assign MPI addresses greater than ”2” to the fixed nodes in the MPI network.
- Reserve the MPI address ”0” for a service PD and ”1” for a service OP which, if necessary, can be connected to the MPI network at short notice.
- Reserve the MPI address ”2” for a CPU. This prevents double MPI addresses occurring when a CPU with default settings is installed in the MPI network (e.g. when a CPU is exchanged).

Startup without configuration on the Micro Memory Card (MMC) (initial startup)

Following POWER ON, the coexistent interface on the BM 147 CPU powers up as an MPI interface with the address 2, HSA 31 and 187.5 kBaud. All PD functions listed in Section 3.4 are possible with the interface.

Note

The bus parameters are retentive, i.e. bus parameters that have been configured (e.g. address, transmission rate) are retained

- with POWER OFF
- if there is no longer a configuration on the BM 147 CPU (e.g. after SDBs have been deleted or following POWER ON without MMC)

Startup with configuration on the Micro Memory Card (MMC)

As soon as a configuration has been downloaded to the BM 147 CPU, the data stored on the MMC is used on startup.

Installation and Wiring

5

The general rules and specifications for mounting and wiring an ET 200X are found in the corresponding chapters of the *ET 200X Distributed I/O Device* manual. The special features of the BM 147 CPU are described here.

Connecting to protective ground

Basic module BM 147 CPU must be connected to protective ground. The basic module is equipped with a grounding screw for this purpose.

Minimum cross section of the cable to protective ground: 4 mm^2

The connection to protective ground is also required for discharging interference currents and for EMC immunity. To improve EMC, it is advisable to select a cross section for the cable to protective ground that is as large as possible (e.g. braided copper cable). The cable should be kept as short as possible.

Note

Ensure that your connection to protective ground is low-impedance.

Figure 5-1 shows how basic modules BM 147 CPU have to be connected to protective ground.

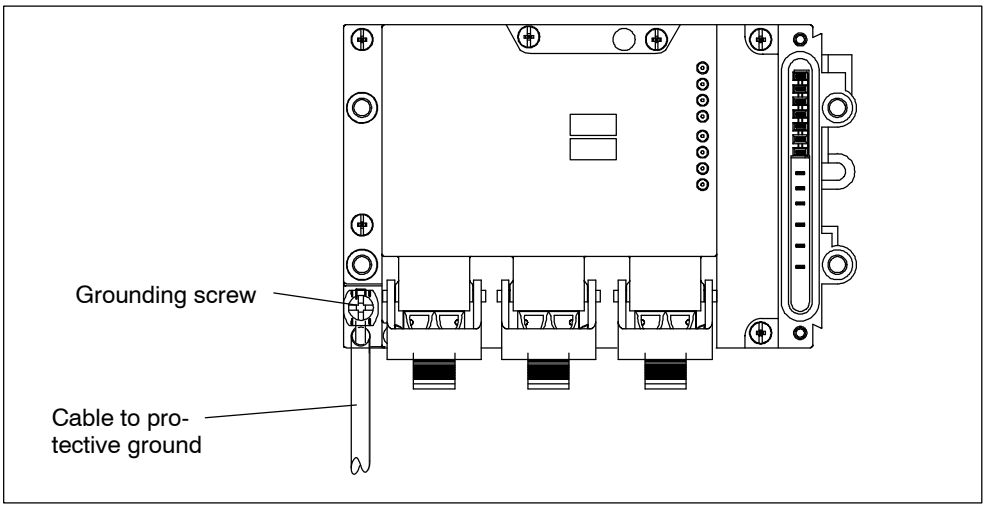


Figure 5-1 Connecting basic module BM 147-2 CPU to protective ground

Interface locations

Figure 5-2 shows where the interfaces are located on the BM 147 CPU.

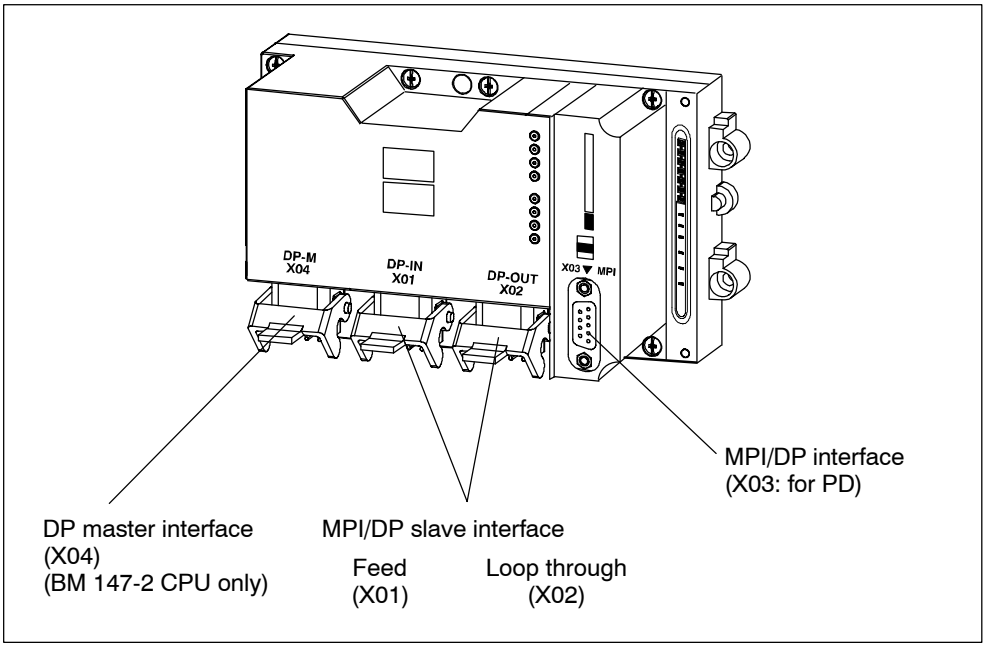


Figure 5-2 Interfaces on basic module BM 147 CPU

Mounting the connectors on BM 147 CPU

Prerequisite

The cables have been wired to the connectors.

Proceed as follows:

1. On the basic module, push the lock for the ECOFAST connectors upward.
2. Plug the ECOFAST connector (non-switched supply voltage (1L+) and the switched load voltage (2L+) and PROFIBUS-DP via copper cable) into the socket on the basic module. Note the mechanical coding of the connectors for feed and looping-through connections.
   Note: To ensure that the degrees of protection IP 65, IP 66 and IP 67 are met, you must always connect all 3 ECOFAST connectors to the basic module. If an ECOFAST socket remains unused, it must be closed off with a cap. The order number for the cap is found in the Appendix A.
3. Push the lock for the ECOFAST connectors downward.

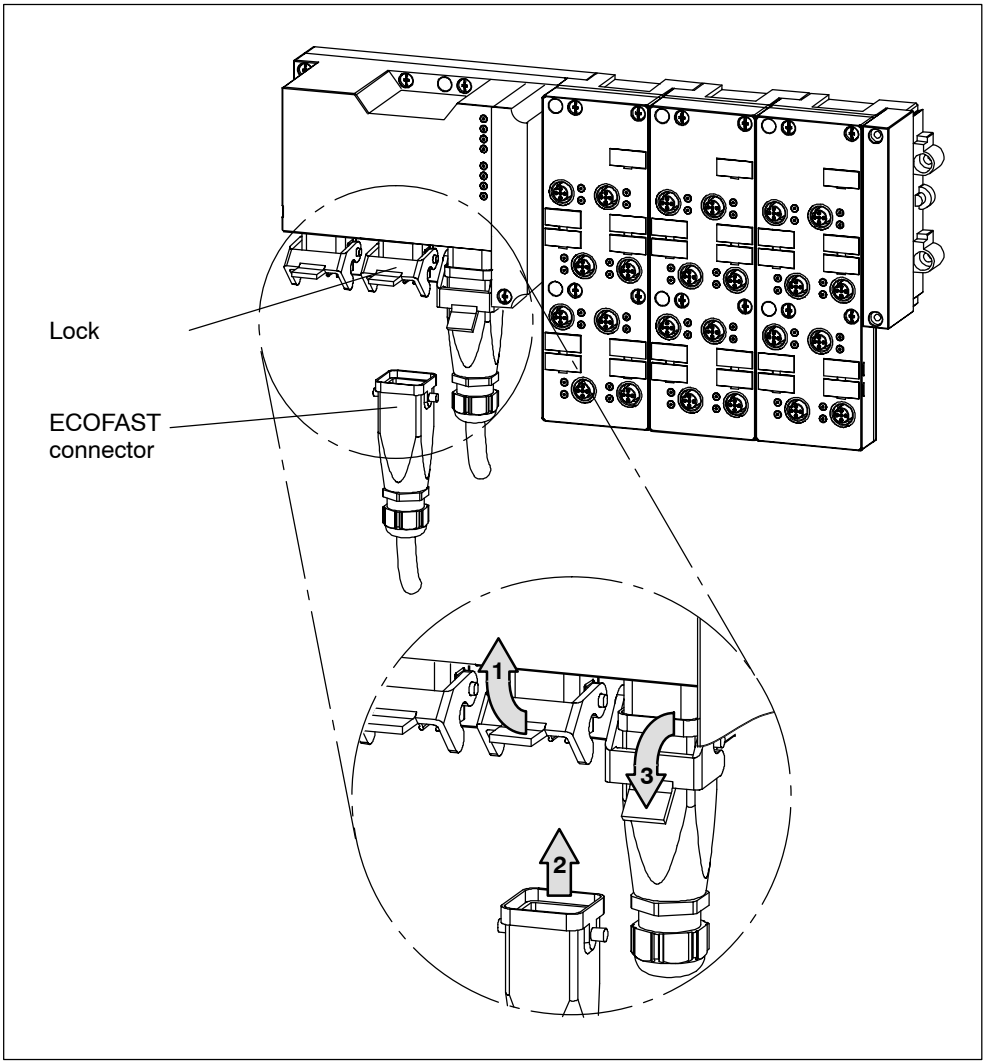


Figure 5-3 Plugging the connector into the BM 147 CPU

Caution

The ECOFAST connectors must not be unplugged during operation of the ET 200X with the BM 147 CPU as this may damage or destroy the modules. Therefore, switch off the non-switched supply voltage (1L+) and the switched load voltage (2L+) as well as the load supply before detaching the connectors!

Terminating the PROFIBUS with a resistor

A bus cable with copper lines must be terminated at the first and last node of the network with its characteristic impedance.

If an ET 200X with BM 147 CPU is the first or last node in a PROFIBUS network, the following procedure must be followed:

- Connect the bus nodes using ECOFAST hybrid cables with copper lines (bus hardware RS 485).
- For the first and last bus node, plug the terminating resistor into the right-hand ECOFAST connector (DP-OUT/X02) of each basic module BM 147 CPU.

The order number for the terminating resistor is found in the Appendix A.

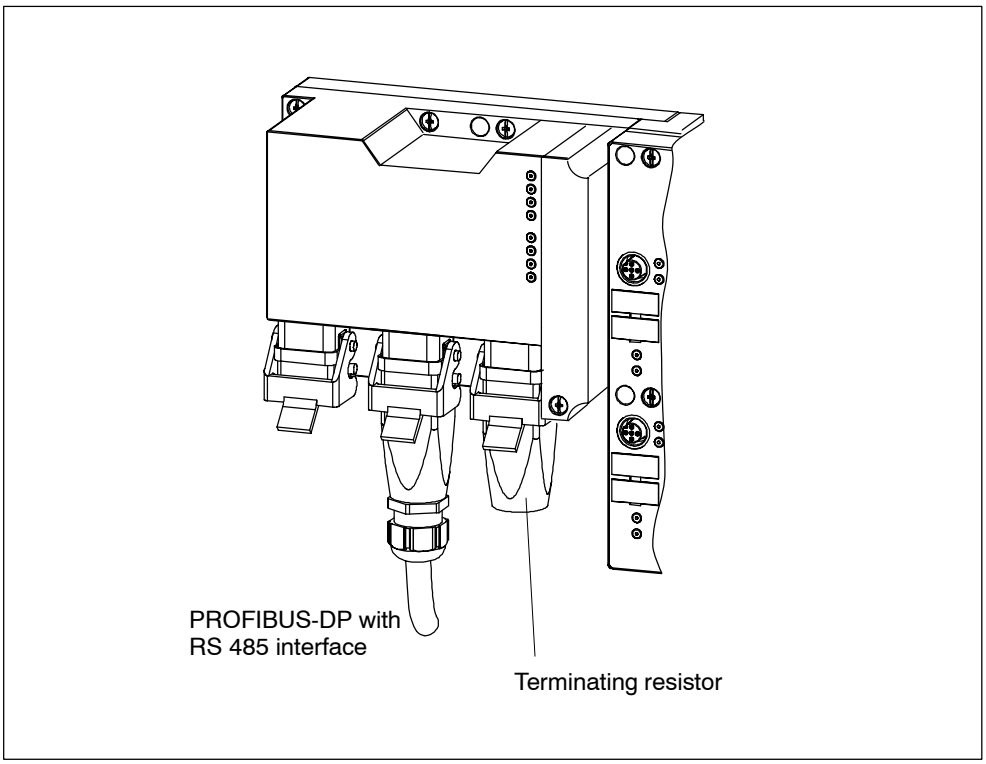


Figure 5-4 Plugging in the terminating resistor

Note

The terminating resistor is supplied by the non-switched supply voltage (1L+). The terminating resistor can only be guaranteed to function properly if the non-switched supply voltage (1L+) has a tolerance range of ±10 %.

Fuse for non-switched supply voltage (1L+)

To protect the modules against overload, the BM 147 CPU is equipped with a fuse for the non-switched supply voltage (1L+).

After blowing of a fuse, the BM 147 CPU behaves as follows:
If the fault that led to the fuse blowing (e.g. short circuit at a sensor) is eliminated, the fuse recovers and the BM 147 CPU runs up again.

Commissioning and Diagnostics

6

Configuring the BM 147 CPU as a DP slave with *STEP 7*

An ET 200X with BM 147 CPU is configured differently from an ET 200X with BM 141 or BM 142. Therefore, this chapter briefly describes how to configure a BM 147 CPU with *STEP 7*.

Resetting the memory of the BM 147 CPU

In certain situations you must reset the memory of the BM 147 CPU. This chapter describes these circumstances and the procedure for resetting the memory of the CPU component.

Diagnostic options

The ET 200X distributed I/O device is designed to make handling and commissioning as simple as possible. If a fault or an error should occur in spite of this, you can analyze it using the LEDs, the slave diagnosis and the diagnostic options in *STEP 7*.

Interrupt evaluation

To help you evaluate the **interrupts** of the ET 200X, we will examine the difference between these and the interrupts of the S7/M7 DP master and other DP masters.

Chapter overview

6.1 Configuring the BM 147 CPU

Configure the basic module BM 147 CPU as an intelligent DP slave or as a standalone module (MPI) and/or as a DP master (BM 147-2 CPU).

The BM 147 CPU is presented to the user in *STEP 7* as an S7-300 module that is always created together with a rack in an S7-300 station. Similarly, the module can only be deleted with the rack!

Expansion racks cannot be configured in an S7-300 station that contains a BM 147 CPU. The BM 147 CPU is connected to slot 2 and obtains an MPI/DP submodule (BM 147-2 CPU also obtains a DP master submodule). The first plug-in modules (maximum of 7) can be configured beginning with slot 4.

The following configuration options are available:

Table 6-1 Configuration options

Configuration environment	Configuration tool	Configurable operating mode
SIMATIC S7	*STEP 7* (HWConfig) V5.2 or higher + Service Pack 1	• Stand-alone (MPI) • BM 147 CPU as S7 slave • BM 147-2 CPU as DP master
SIMATIC S5	COM PROFIBUS	Fully configured and programmed BM 147 CPU, integrated as a standard intelligent slave via GSD in COM PROFIBUS
Non-Siemens systems	Non-Siemens tool	Fully configured and programmed BM 147 CPU, integrated as a standard intelligent slave via GSD in a non-Siemens tool

Note

If you wish to operate the BM 147 CPU as a standard slave via the GSD file, then you should not activate the commissioning/test mode checkbox in the DP interface properties when configuring this slave CPU in *STEP 7*.

Prerequisite

You have opened STEP *7* (V5.2 or higher + Service Pack 1) and are in the SIMATIC Manager of *STEP 7*.

Configuring the BM 147 CPU as a DP slave

Proceed as follows:

1. Configure the BM 147 CPU as an S7-300 station.
   - Create a new station of the type **S7-300** (menu command **Insert** → **Station**).
   - Change to the hardware configuration window for this station.
   - In the “Hardware Catalog” window, select the PROFIBUS-DP/ET 200X/BM 147 CPU folder.
   - Drag and drop the “BM 147 CPU” object in the empty station window.
   - Configure the ET 200X with the required expansion modules.
   - Save the station (i.e. the ET 200X).
2. Configure a DP master (e.g. CPU with integrated PROFIBUS-DP interface or CP 342-5 with PROFIBUS-DP interface as of 6GK7 342-5DA01-0XE0, version 2) in another station in the same project.
3. Drag the ET 200X (with the BM 147 CPU) from the “Hardware Catalog” window (from the **configured stations**) and drop it the icon for the DP master system.
4. Double-click the intelligent DP slave icon, and select the ”Interconnecting” tab. Specify on this tab which station is to represent the intelligent DP slave.
5. Select the intelligent DP slave, and click the ”Interconnect” button.
6. Select the (slave) configuration tab, and assign the master and slave addresses.
7. Click ”OK” to accept the settings.
8. The two stations must then be reloaded to start master-slave communication.

Configuration in a non-Siemens system

Using the DDB file you can also integrate the BM 147 CPU in non-Siemens systems as a DP standard slave. In this case the diagnostic frame consists of the following:

- Station status
- Master PROFIBUS address
- Manufacturer ID
- Module diagnostics
- Module status

Configuring the BM 147-2 CPU as a DP master

The BM 147-2 CPU must be configured as a DP master. This means that you have to configure interface X04 of the BM 147-2 CPU as a DP master in *STEP 7*,

- assign the BM 147-2 CPU a PROFIBUS address,
- assign the BM 147-2 CPU a master diagnosis address,
- integrate DP slaves in the DP master system.

  Is a BM 147 CPU a DP slave?
  Then you will find this DP slave in the PROFIBUS-DP catalog as a **pre-configured station**. In the DP master, you assign a slave diagnosis address to this DP slave CPU. You have to couple the DP master with the DP slave CPU and define the address ranges for the data exchange with the DP slave CPU.

6.2 Resetting the memory of the BM 147 CPU

When do you reset the memory of the BM 147 CPU?

The memory of the BM 147 CPU must be reset

- to erase retentive areas (memory markers, times, counters)
- if the BM 147 CPU requests a memory reset by flashing the STOP LED at 0.5 Hz

The following are possible reasons for the MRES request:

- The ET 200X is starting up for the first time.
- Inconsistent memory areas
- The memory module (MMC) has been replaced.

How do you reset the memory?

There are two ways of resetting the BM 147 CPU:

Table 6-2 Ways to reset the memory

Resetting the memory with the mode selector	Resetting the memory with the PD
Described in this chapter.	Only possible during CPU STOP (see the PD manuals and the *STEP 7 Online Help*)

Resetting the memory of the BM 147 CPU with the mode selector

To reset the memory of the BM 147 CPU using the mode selector, proceed as follows (see also Figure 6-1):

1. Undo the screws on the front panel (captive cross-recessed screws) and open the panel upwards.
2. Switch the mode selector to the STOP position.
3. Depress the mode selector in the MRES position. Hold the mode selector at this position until the STOP LED lights up for the second time (3 seconds) and then let it return to the STOP position.
4. Within 3 seconds, you must press the mode selector back to the MRES position and hold it in this position until the STOP LED flashes rapidly (at 2 Hz). When the BM 147 CPU has completed the memory reset, the STOP LED stops flashing and remains on.
5. Select the required operating mode (RUN/STOP).
6. Close the front panel again and screw it shut.

The BM 147 CPU has reset the memory.

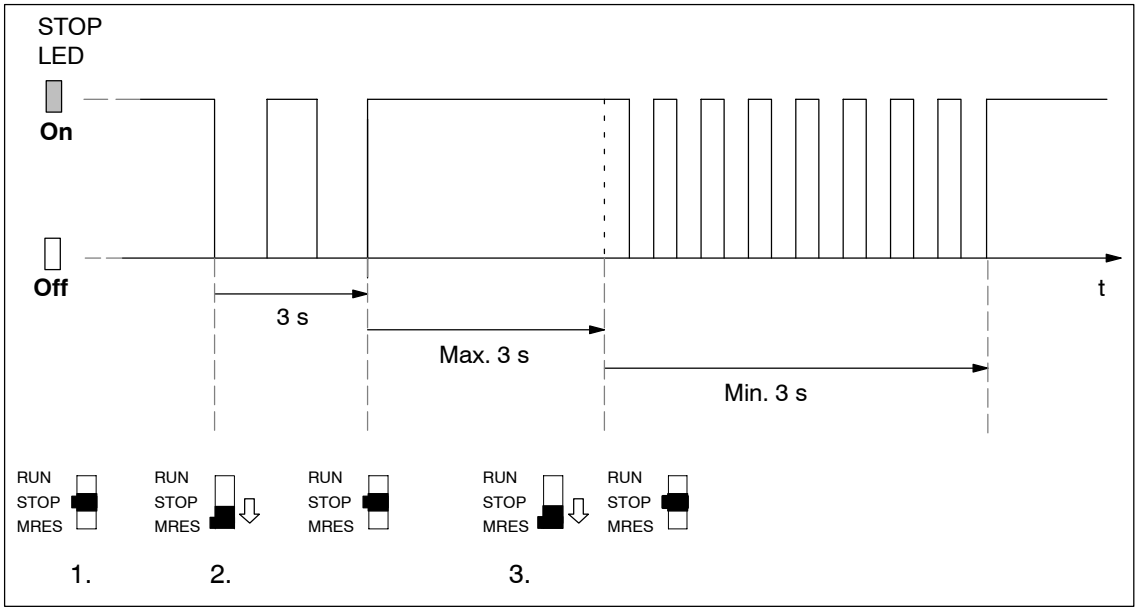


Figure 6-1 Operating sequence on the mode selector for performing a general reset

Is the STOP LED not flashing at memory resetting?

Does the STOP LED not flash during memory reset or do other indicators come on? You must repeat steps 3 and 4. If the BM 147 CPU again does not carry out the memory reset, you must read out the diagnostic buffer of the CPU using the programming device (see the *STEP 7 user manual*).

What happens in the BM 147 CPU?

Table 6-3 Internal CPU events at memory resetting

Event	Response of the CPU in the BM 147 CPU
Sequence of operations in the BM 147 CPU	1. The CPU deletes the entire user program in the working memory and the RAM load memory. 2. The CPU deletes the retentive data. 3. The CPU tests its own hardware. 4. If you have inserted a memory module (micro memory card = MMC), the CPU copies the relevant contents of the module to the working memory.
Memory contents after reset	The CPU has the memory level ”0”. If a SIMATIC micro memory card is inserted, the user program is transferred back into the working memory.
What’s left?	The contents of the diagnostic buffer and the runtime meter.

Note

If the CPU cannot copy the contents of the memory module (MMC) and requests a memory reset:

- Remove the MMC.
- Reset the CPU memory.
- Read out the diagnostic buffer.

You can read out the diagnostic buffer with the PD (see the *STEP 7 Online Help*).

6.3 Commissioning and start-up of the ET 200X

6.3.1 Starting up the BM 147 CPU as a DP slave

Commissioning the ET 200X

Commission the ET 200X distributed I/O device as follows:

1. Install the ET 200X distributed I/O device
   (see the *ET 200X Distributed I/O Device manual)*).
2. Wire the ET 200X distributed I/O device
   (see Chapter5 and the *ET 200X Distributed I/O Device*) manual.
3. During configuration as a DP slave, specify in the configuration software the address areas in the BM 147 CPU via which data exchange with the DP master is to take place (or use the ET 200X default setting; see Section 2.4).
4. Switch on the non-switched supply voltage for the electronics/sensors (1L+) and the switched load voltage (2L+) for the ET 200X.
5. If necessary, switch on the load voltage and the load supply voltage for the motor starters.
6. If necessary, switch the BM 147 CPU to STOP mode.
7. Load the configuration for the BM 147 CPU in the ET 200X.
8. Switch the BM 147 CPU to RUN mode.

Setting the bus parameters for the PROFIBUS-DP in *STEP 7*

Note

To comply with the values required for electromagnetic compatibility, you must set the following bus parameter in *STEP 7* **for the 500 kBaud and 1.5 MBaud baudrates**:

"Retry Limit" to at least "3"

Leave all the other bus parameters as they are, in accordance with your selected bus profile.

Tip: Programming OB 82 and 86 during commissioning

Always program OB 82 and OB 86 when commissioning as a DP slave in the DP master and DP slave using *STEP 7*. This will allow you to detect and evaluate the operating states of and interruptions during user data transfer (see Tables 6-7 and 6-8).

Note

Without configuration, a default start-up is possible if the power modules are switched on and all the modules are inserted.

6.3.2 Starting up the BM 147-2 CPU as a DP master

Commissioning

Commission the BM 147-2 CPU as a DP master in the PROFIBUS subnet as follows:

1. Switch the supply voltage on.
2. Load the configuration of the PROFIBUS subnet (preset configuration) created with *STEP 7* into the BM 147-2 CPU with the PD.
3. Switch all DP slaves on.
4. Switch the BM 147-2 CPU from STOP to RUN mode.

Initializing the DP master system

In addition, the initialization time monitor for the DP slave can be set with the **Monitoring time for transfer of parameters to modules** parameter.

This means that the DP slaves must be initialized and parameterized by the BM 147-2 CPU (as DP master) within the set time period.

Start-up of the BM 147-2 CPU as a DP master

When it starts up, the BM 147-2 CPU compares the preset configuration of the DP master system with the actual configuration.

If the preset configuration = the actual configuration, the CPU goes into RUN mode.

If the preset configuration ≠ the actual configuration, the behavior of the CPU depends on the setting of the **Start-up when the preset configuration ≠ actual configuration** parameter.

Start-up when preset configuration ≠ actual configuration = yes (default setting)	**Start-up when preset configuration ≠ actual configuration = no**
BM 147-2 CPU goes into RUN mode. (BF-LED on the DP master module flashes if all DP slaves cannot be addressed.)	BM 147-2 CPU remains in STOP mode and the BF-LED on the DP master module flashes after the set **Monitoring time for transfer of parameters to modules** has elapsed. A flashing BF-LED indicates that at least one DP slave cannot be addressed. Check whether all DP slaves are switched on and that they correspond to the defined configuration, or read out the diagnostic buffer using *STEP 7*.

Recognizing the operating modes of the DP slave (event recognition)

The table below shows how the BM 147-2 CPU identifies changes in operating mode and interruptions in data transfer as a DP master.

Table 6-4 Event recognition of the BM 147-2 CPU as a DP master

Event	What takes place in the DP master?
Bus interruption (short-circuit, connector removed)	• OB 86 is called and **Station failure** is reported (incoming event; diagnosis address of the DP slave assigned to the DP master) • In the case of I/O access: OB 122 is called (I/O access error)
DP slave: RUN → STOP	• OB 82 is called and **Module malfunction** reported (incoming event; diagnosis address of the DP slave assigned to the DP master; variable OB82_MDL_STOP=1)
DP slave: STOP → RUN	• OB 82 is called and **Module ok** reported. (outgoing event; diagnosis address of the DP slave assigned to the DP master; variable OB82_MDL_STOP=0)

Tip:
Always program OB 82 and OB 86 when commissioning the CPU as a DP master. This will allow you to detect and evaluate the faults and interruptions during data transfer.

Status/controlling, programming via PROFIBUS-DP

You can program the CPU or execute the PD functions listed in Chap. 3.4 via the DP master interface.

Note

The use of status and control via the DP master interface extends the DP cycle.

Equidistance

As of *STEP 7* V 5.2 + SP1, you can parameterize bus cycles of the same length (equidistant) for PROFIBUS subnets with BM 147 CPU. You will find a detailed description of the functions in the *Online Help for STEP 7*.

PROFIBUS address of the DP master

- The permitted PROFIBUS-DP addresses are 1 to 125.
- Each address can be allocated only once on the PROFIBUS-DP.

6.3.3 Start-up

Loading the user program

When commissioning the ET 200X, you can download the user program to the BM 147 CPU in the following ways:

- The program is downloaded from the PD/PC to the memory module (MMC) inserted in the BM 147 CPU by means of the ”Load user program” function.

Note

This function does not delete retentive areas.

- The program is transferred from the PD/PC to the memory module (MMC). The memory module is then inserted in the BM 147 CPU and the memory reset request acknowledged.

See Section 7.3.

Start-up

When the BM 147 CPU is switched to RUN mode, the following mutually independent operating mode transitions take place:

- The CPU switches from STOP to RUN mode.
- The BM 147 CPU starts user data transfer with the DP master on the PROFIBUS-DP.
- The BM 147-2 CPU starts user data transfer with the DP slaves on the PROFIBUS-DP.

6.4 Diagnostics using LEDs

LEDs

The LEDs RUN, STOP, ON, 24 VDC, BF-S, BF-M, SF and FRCE display important information on the states of the BM 147 CPU.

The BM 147 CPU has the following 8 LEDs:

- ”SF” LED (**S**ystem **F**ault) for indicating the presence of a fault in the ET 200X
- LEDs “BF-S” and “BF-M” (**B**us **F**ault) for indicating the presence of faults in the PROFIBUS-DP (“BF-M” only for BM 147-2 CPU)

  BF-S: Bus fault on slave strand
  BF-M: Bus fault on master strand
- LED “ON” for indicating that the ET 200X is connected to a non-switched supply voltage for electronics/sensors (1L+)
- LED “24 VDC” for indicating that the ET 200X is connected to a switched load voltage (2L+)
- ”FRCE” LED for indicating that a force request is active.
- “RUN” LED for indicating that the BM 147 CPU is in RUN mode
- “STOP” LED for indicating that the BM 147 CPU is in STOP mode

The meaning of the LEDs for CPU functionality is described in detail in Section 7.2.

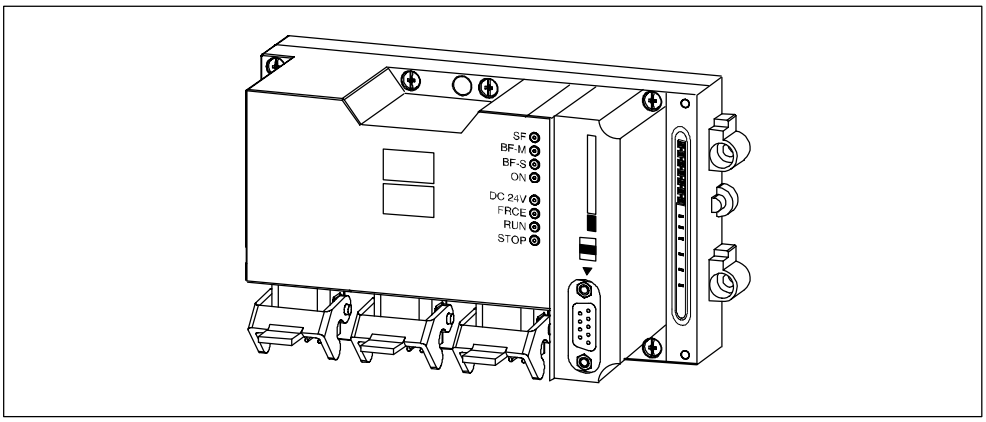


Figure 6-2 Position of LEDs on basic module BM 147 CPU

”ON” LED is Off

If the ”ON” LED is off, either no supply voltage or insufficient non-switched supply voltage is being applied to the electronic components/sensors (1L+) of the ET 200X. The cause is likely to be a defective fuse or inadequate or nonexistent system voltage.

Diagnosis of DP functionality using the ”BF-S”, ”BF-M” and ”SF” LEDs

If the ”BF-S”, ”BF-M” and ”SF” LEDs light up or flash, the ET 200X is not configured correctly. The tables below shows you the possible error indications together with their meanings and the necessary action.

The table 6-5 shows the LED states for DP slave operation. DP functionality is irrelevant in stand-alone operation (MPI), and a BF-S LED is not activated (there is no LED for transmission rate detection).

Table 6-5 LED display for PROFIBUS-DP (BM 147 CPU is a slave)

LED “BF-S”	”SF” LED	Description	Cause	Error handling
On	On	No connection to the DP master	• BM 147 CPU is the active node ⇒ Bus short-circuit • BM 147 CPU is the passive node ⇒ Transmission rate detection: No active node at bus, DP master does not exist or is switched off, or bus connection interrupted • Bus connection interrupted • Master does not exist or is switched off SF is on due to station failure	• Check that the connector for the PROFIBUS-DP is inserted correctly • Check whether the bus cable to the DP master is defective
Flashing	On	Parameter assignment error; there is no data exchange	• Slave not configured or incorrectly configured • Incorrect but permissible station address configured • Configured address areas of the actual configuration not identical to the target configuration • Station failure of a configured sender in direct data communication • DP master not present or switched off (only applies if the BM 147 CPU is a passive bus note and there are no other active bus nodes other than the PD/OP)	• Check the hardware of the ET 200X • Check the configuration and parameterization of the ET 200X • Check the setting for the configured address areas for the master
Off	On	Fault in slave: Diagnostic interrupt	Master in STOP	Switch the DP master to RUN mode.
Off	Off	Data exchange taking place	The target configuration and actual configuration of the ET 200X match.	

The table 6-6 shows the LED states for DP master operation.

Table 6-6 LED display for PROFIBUS-DP (BM 147-2 CPU is a master)

LED “BF-M”	”SF” LED	Description	Cause	Error handling
On	On	No connection to the DP slave	• Bus connection interrupted • Slave does not exist or is switched off • Bus short-circuit	• Check that the connector for the PROFIBUS-DP is inserted correctly • Check whether the bus cable to the DP master is defective • Evaluate the diagnosis. Reconfigure or correct the configuration.
Flashing	On	• There is no data exchange • Parameter assignment error	• A connected station has failed • At least one of the assigned slaves cannot be addressed • Configured address areas of the actual configuration not identical to the target configuration	• Check whether the bus cable is connected to the CPU or the bus is interrupted. • Wait until the CPU has run up. If the LED does not stop flashing, check the DP slaves or evaluate the diagnosis of the DP slaves. • Check the setting for the configured address areas for the master

6.5 Diagnostics via diagnostic address with *STEP 7*

Malfunctions that occur in the ET 200X are indicated by the “SF” LED, and the cause is entered in the diagnostic buffer of the BM 147 CPU. Either the CPU enters STOP mode, or you can respond to errors by means of error or interrupt OBs in the user program.

To enable a response to be made, it must be possible to identify whatever caused the problem by means of a diagnostic address.

Diagnostic addresses

If you run the ET 200X with a DP master from the SIMATIC S7 range on the PROFIBUS-DP, diagnostic addresses are assigned in *STEP 7* as follows:

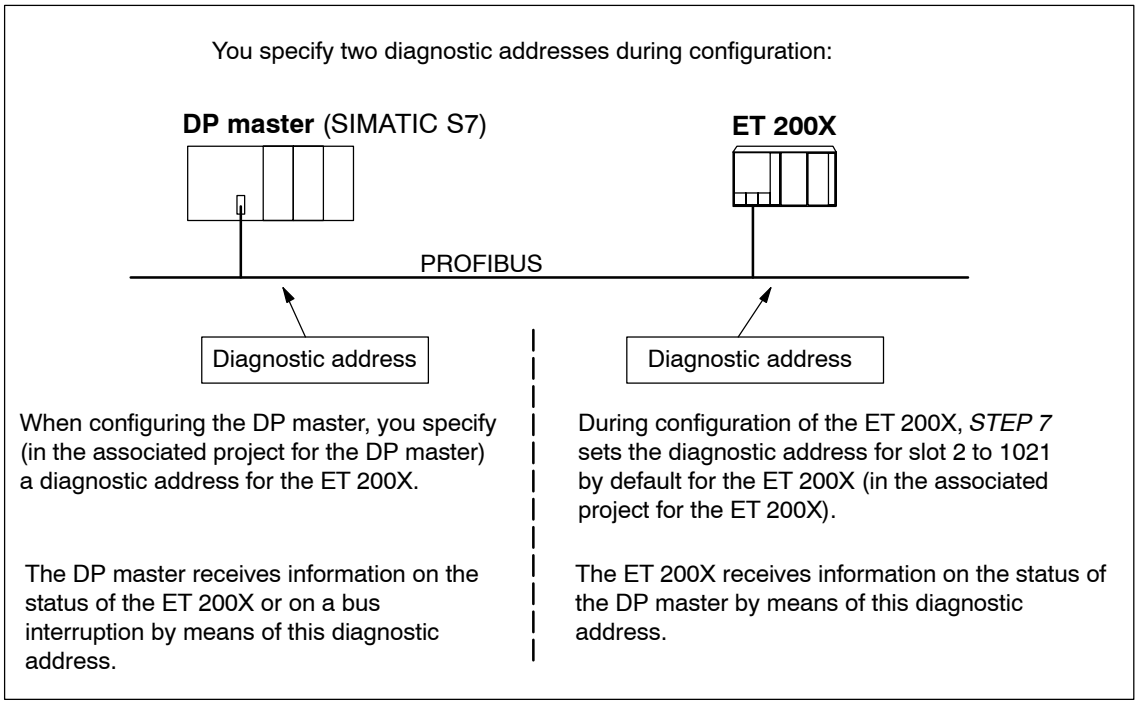


Figure 6-3 Diagnostic addresses for the DP master and ET 200X

Event identification

The following table indicates how the DP master or the BM 147 CPU of the ET 200X identifies changes in operating mode and interruptions in user data transfer.

Table 6-7 Responses to operating mode changes and interruptions in user data transfer in the DP master and the ET 200X with the BM 147 CPU

Event	What happens ...	
	in the DP master	in the BM 147 CPU
Bus interruption (short-circuit, connector removed)	• OB 86 is called with the message *Station failure* (incoming event; diagnostic address of the BM 147 CPU) • With I/O access to transfer area: OB 122 is called (I/O access error)	• OB 86 is called with the message *Station failure* (incoming event; diagnostic address of the BM 147 CPU) • With I/O access to transfer area: OB 122 is called (I/O access error)
ET 200X: RUN → STOP	• OB 82 is called with the message *Faulty module* (incoming event; diagnostic address of the BM 147 CPU; variable OB82_MDL_STOP=1)	–
ET 200X: STOP → RUN	• OB 82 is called with the message *Module ok.* (outgoing event; diagnostic address of the BM 147 CPU; variable OB82_MDL_STOP=0)	–
DP master: RUN → STOP	–	• OB 82 is called with the message *Faulty module* (incoming event; diagnostic address of the BM 147 CPU; variable OB82_MDL_STOP=1)
DP master: STOP → RUN	–	• OB 82 is called with the message *Module ok.* (outgoing event; diagnostic address of the BM 147 CPU; variable OB82_MDL_STOP=0)

Evaluation in the user program

The table below indicates how you can evaluate e.g. RUN-STOP transitions in the DP master (CPU 315-2 DP; 6ES7 315-2AF03-0AB0) and in the ET 200X.

Table 6-8 Evaluation of RUN/STOP Transitions in the DP Master/ET 200X

In the DP master		In the ET 200X (BM 147-1 CPU)
Diagnostic addresses: (example) Master diagnostic address=1023 Slave diagnostic address in the master system=**1022**		Diagnostic addresses: (example) Slave diagnostic address, slot 2=**1021** Master diagnostic address=not relevant
The CPU calls OB 82 with the following information: • OB 82_MDL_ADDR:=**1022** • OB82_EV_CLASS:=B#16#39 (incoming event) • OB82_MDL_DEFECT:=Module fault Tip: This information is available in the diagnostic buffer of the CPU. In the user program, you should also program SFC 13 (”DPNRM_DG”) to read out the slave diagnosis.	←	CPU in the BM 147 CPU: RUN → STOP The CPU generates a diagnostic frame (slave diagnosis; see the *ET 200X Distributed I/O Device* manual).
CPU: RUN → STOP	→	The BM 147 CPU calls OB 82 with information including the following: • OB 82_MDL_ADDR:=**1021** • OB82_EV_CLASS:=B#16#39 (incoming event) • OB82_MDL_DEFECT:=Module fault Tip: This information is available in the diagnostic buffer of the CPU.

6.6 Slave diagnostics with BM 147 CPU as intelligent slave

Structure of the diagnostic frame

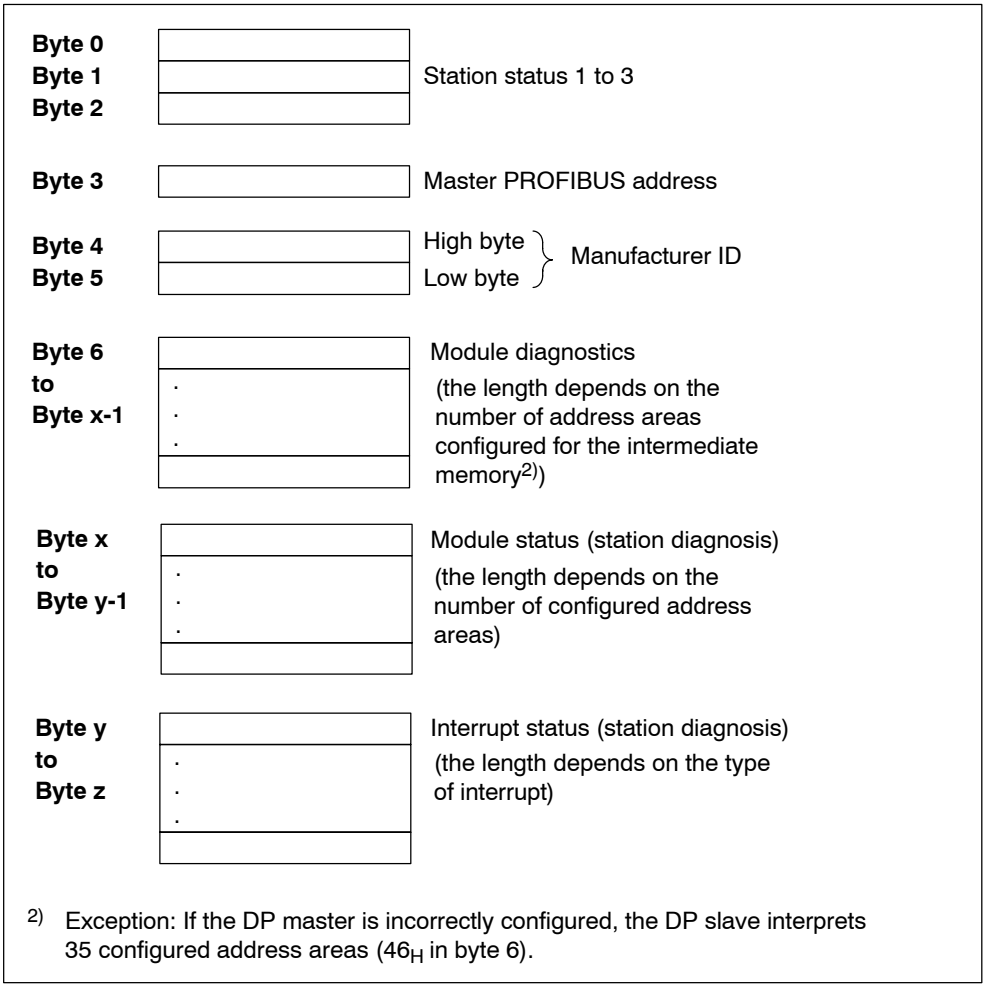


Figure 6-4 Format of the slave diagnostic data

6.6.1 Station status 1 to 3

Definition

Station status 1 to 3 provides an overview of the status of a DP slave.

Station status 1

Table 6-9 Structure of station status 1 (byte 0)

Bit	Description	Remedy
0	1: DP slave **cannot** be addressed by DP master.	• Is the correct DP address configured for the DP slave? • Is the bus connector inserted? • Does the DP slave have power? • Is the RS 485 repeater correctly set? • Execute a reset on the DP slave.
1	1: DP slave is not ready for data interchange.	• Wait; the DP slave is still doing its run-up.
2	1: The configuration data which the DP master sent to the DP slave do not correspond with the DP slave's actual configuration.	• Correct station type or correct configuration of the DP slave entered in the configuration software?
3	1: Diagnostic interrupt, generated by RUN-STOP transition of the CPU or by the SFB 75 0: Diagnostic interrupt, generated by STOP-RUN transition of the CPU or by the SFB 75	• You can read out the diagnostic data.
4	1: Function is not supported, for instance changing the DP address at the software level.	• Check the configuration data.
5	0: This bit is always "0".	–
6	1: DP slave type does not correspond to the software configuration.	• Was the configuration software set for the right station type? (parameter assignment error)
7	1: DP slave was parameterized by a different DP master to the one that currently has access to it.	• Bit is always "1" when, for instance, you are currently accessing the DP slave via the PD or a different DP master. The DP address of the master that parameterized the slave is located in the "Master PROFIBUS address" diagnostic byte.

Station status 2

Table 6-10 Structure of station status 2 (byte 1)

Bit	Description
0	1: DP slave must be parameterized again and reconfigured.
1	1: A diagnostic message has arrived. The DP slave cannot continue operation until the error has been rectified (static diagnostic message).
2	1: This bit is always ”1” when there is a DP slave with this DP address.
3	1: The watchdog monitor has been activated for this DP slave.
4	1: DP slave has received ”FREEZE” control command.
5	1: DP slave has received ”SYNC” control command.
6	0: The bit is always at 0.
7	1: DP slave is deactivated, that is to say, it has been removed from the scan cycle.

Station status 3

Table 6-11 Structure of station status 3 (byte 2)

Bit	Description
0 to 6	0: These bits are always ”0”.
7	1: • More diagnostic messages have arrived than the DP slave can buffer. • The DP master cannot enter all the diagnostic messages sent by the DP slave in its diagnostic buffer.

6.6.2 Master PROFIBUS address

Definition

The DP address of the DP master is stored in the master PROFIBUS address diagnostic byte:

- The master that parameterized the DP slave
- The master that has read and write access to the DP slave

Master PROFIBUS address

Table 6-12 Structure of the master PROFIBUS address (byte 3)

Bit	Description
0 to 7	DP address of the DP master that parameterized the DP slave and has read/write access to that DP slave.
	FF_H: DP slave has not been parameterized by a DP master.

6.6.3 Manufacturer ID

Definition

The manufacturer identification contains a code specifying the DP slave's type.

Manufacturer ID

Table 6-13 Structure of the manufacturer identification (bytes 4 and 5)

Byte 4	Byte 5	Manufacturer identification for
80_H	$F7_H$	BM 147-1 CPU
80_H	$F8_H$	BM 147-2 CPU

6.6.4 Module diagnostics

Definition

The module diagnosis indicates for which of the configured address areas of the intermediate memory an entry has been made.

Structure

The following figure shows the structure of the module diagnosis for the maximum number of configured address areas.

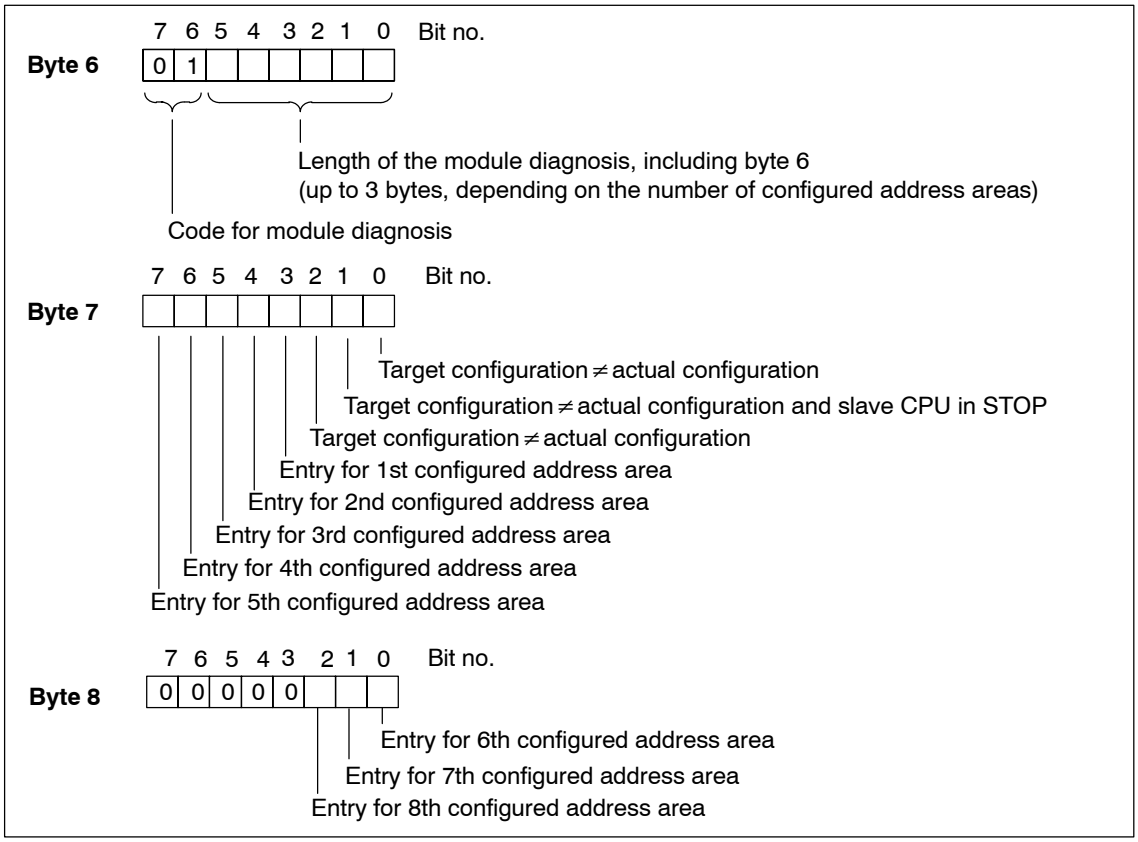


Figure 6-5 Structure of the module diagnosis for the BM 147 CPU

6.6.5 Module status

Definition

The module status indicates the status of the configured address areas and expands on the module diagnosis as regards the configuration. The module status begins after the module diagnosis and comprises max. 7 bytes.

Structure

The module status of the BM 147 CPU is structured as follows:

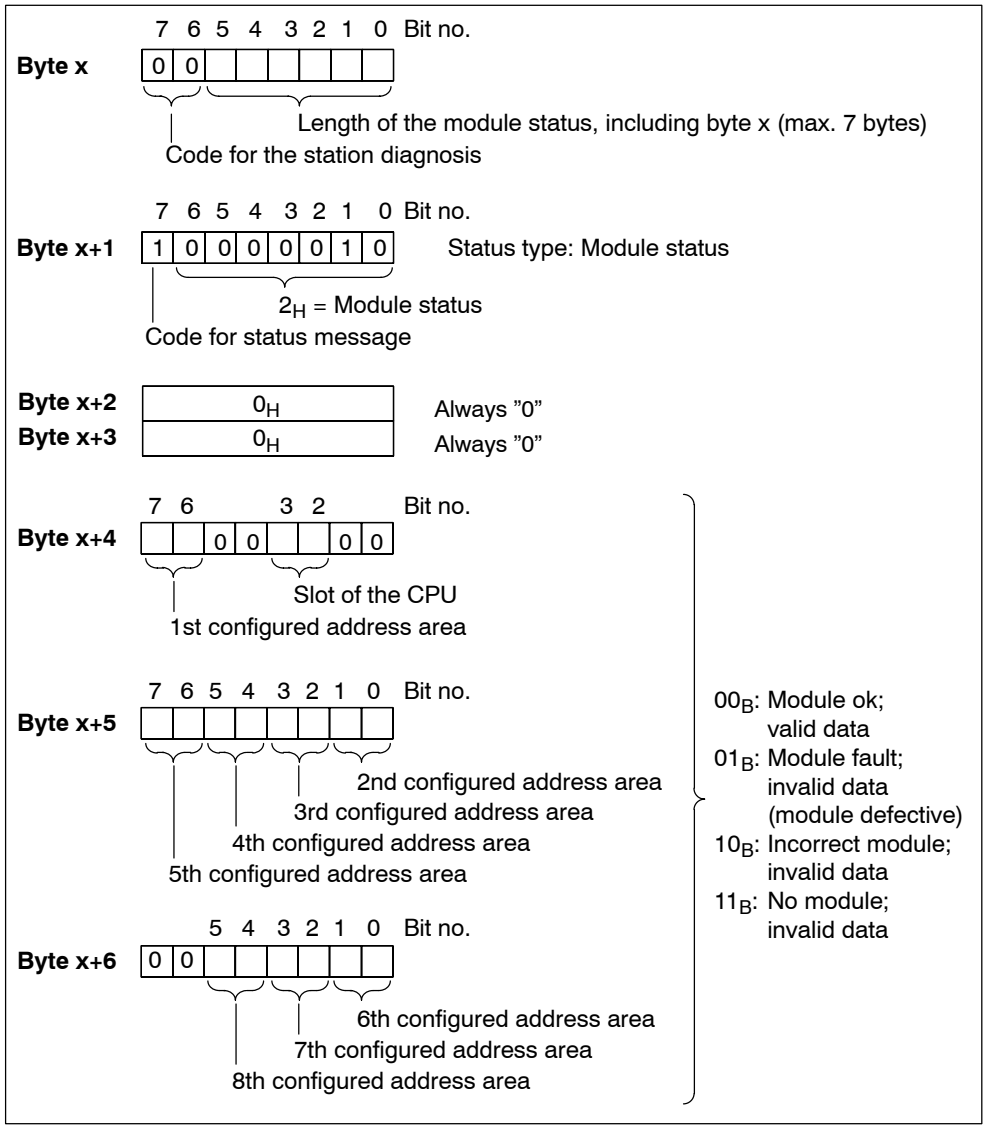


Figure 6-6 Structure of the module status

6.6.6 Interrupt status

Definition

The interrupt status of the station diagnosis provides detailed information about a DP slave. The station diagnosis begins at byte y and can comprise max. 20 bytes. You have 4 bytes available for an interrupt event that you can program as required.

Structure

The following figure shows the structure and content of the bytes for a configured address area of the intermediate memory.

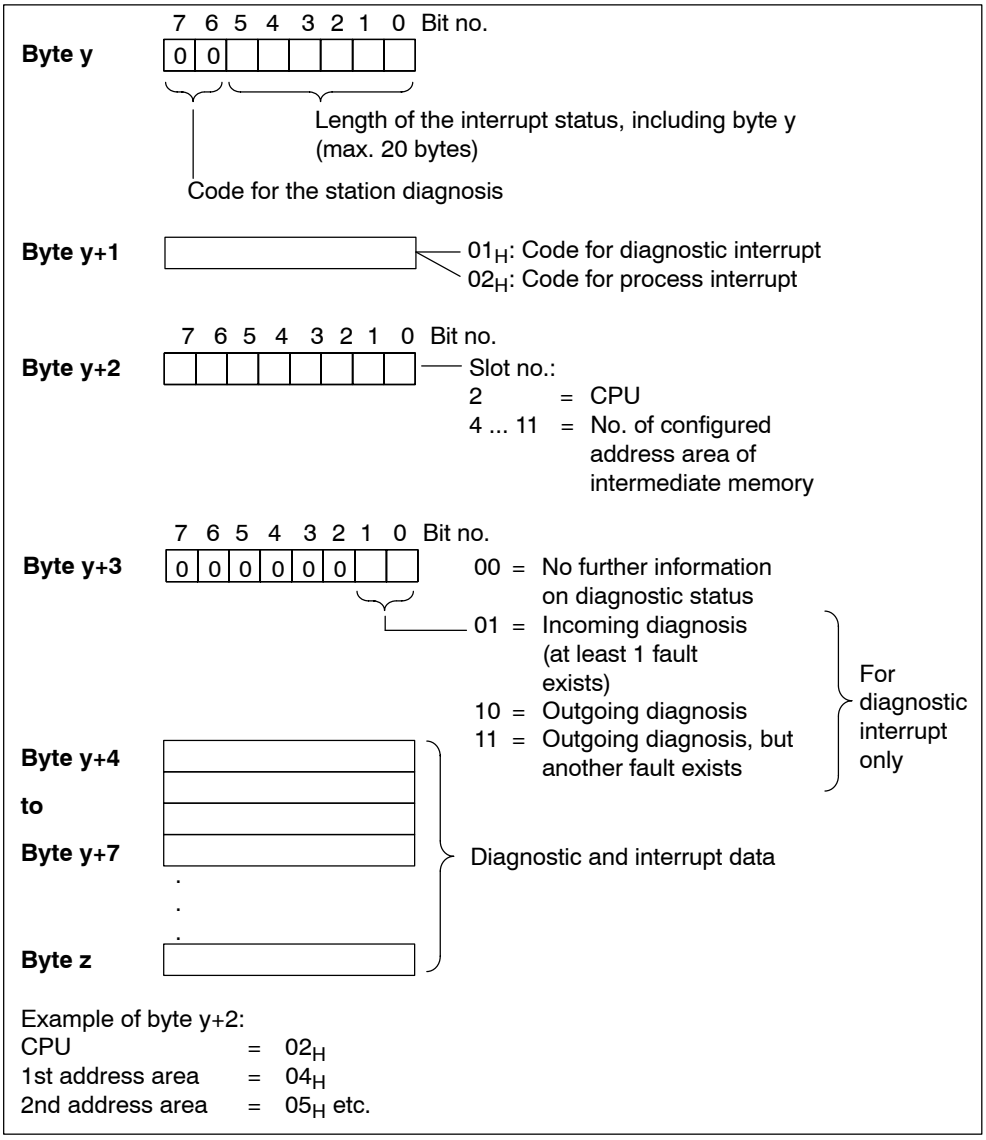


Figure 6-7 Structure of the interrupt status

Structure of the interrupt data with process interrupt (from Byte y+4 onwards)

With the process interrupt (in byte y+1, code 02_H stands for a process interrupt), the 4 byte interrupt information which you transfer in the intelligent slave with the SFC 7 ”DP_PRAL” and SFB 75 ”SALRM” when the process interrupt is generated for the master, is transferred from byte y+4 onwards.

Structure of the interrupt data when a diagnostic interrupt is generated by a mode change at the intelligent slave (from Byte y+4 onwards)

In the byte y+1, the code stands for diagnostic interrupt (01_H). The diagnostic data contains the 16 byte status information for the CPU. The following figure shows the assignment of the first 4 bytes of the diagnostic data. The next 12 bytes are always 0.

The content of these bytes corresponds to the content of data record 0 for diagnosis in *STEP 7* (in this case not all bits are assigned).

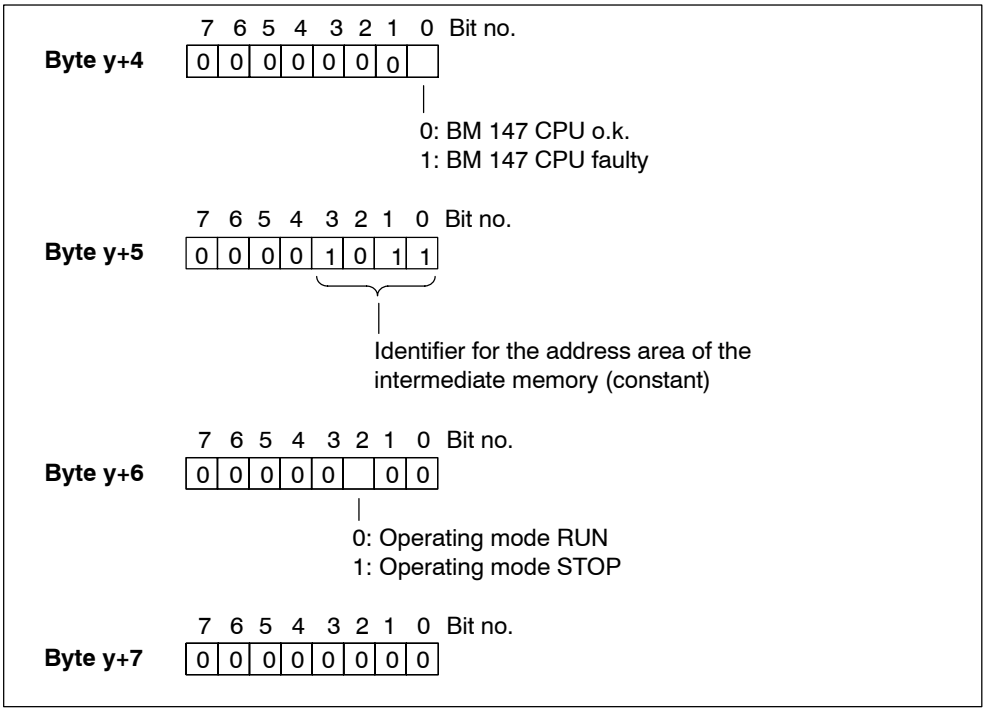


Figure 6-8 Byte y+4 to y+7 for the diagnostic interrupt (changed operating status of the intelligent slave)

Structure of the interrupt data when a diagnostic interrupt is generated by the SFB 75 in the intelligent slave (from Byte y+4 onwards)

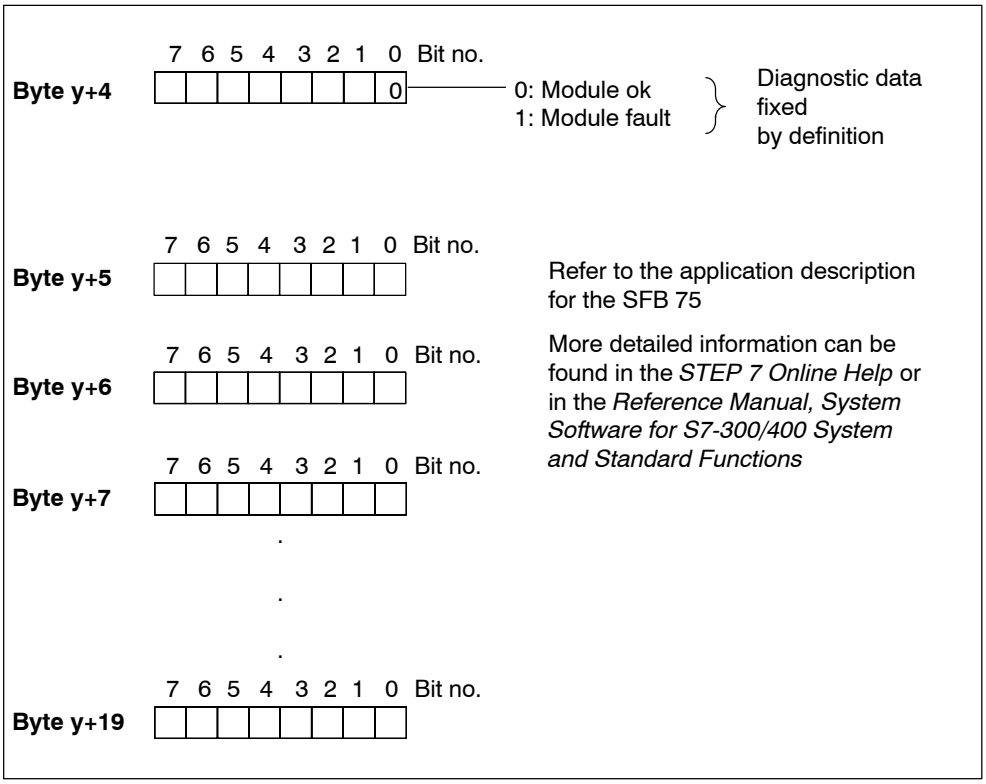


Figure 6-9 Byte y+4 to y+7 for diagnostic interrupt (SFB 75)

Functions of the BM 147 CPU

7

In this chapter

In this chapter you will find:

- Important features of the BM 147 CPU for PROFIBUS-DP
- A list of the CPU functions of the BM 147 CPU that you can call with *STEP 7*, such as the integrated clock, blocks for the user program and parameters that can be set

Chapter overview

7.1 Data for the PROFIBUS-DP

DDB (Device Database) file

A device master file contains all the slave-specific properties. The structure of the DDB file is defined in IEC 61784-1:2002 Ed1 CP 3/1.

You only need the DDB file if:

- You are using the ET 200X with a DP master from the SIMATIC S5 range (configuration with COM PROFIBUS).
- You are using the ET 200X with a non-SIMATIC DP master (configuration with a non-Siemens tool).

You can download the DDB file from the Internet. You will find all the DDB files under ”Downloads” on the SIMATIC Customer Support web site:
`http://www.ad.siemens.de/csi/gsd`

Important features

If you do not have the device master file to hand, the table below lists the most important features of the BM 147 CPU.

Feature	DP code word to IEC 61784-1:2002 Ed1 CP 3/1	BM 147 CPU
Manufacturer ID	Ident_Number	$80F7_H/80F8_H$
Supports FMS	FMS_supp	No
Supports 9.6 kbaud	9.6_supp	Yes
Supports 19.2 kbaud	19.2_supp	Yes
Supports 45.45 kbaud	45.45_supp	Yes
Supports 93.75 kbaud	93.75_supp	Yes
Supports 187.5 kbaud	187.5_supp	Yes
Supports 500 kbaud	500_supp	Yes
Supports 1.5 Mbaud	1.5M_supp	Yes
Supports 3 Mbaud	3M_supp	Yes
Supports 6 Mbaud	6M_supp	Yes
Supports 12 Mbaud	12M_supp	Yes
Supports the FREEZE control command	Freeze_Mode_supp	Yes
Supports the SYNC control command	Sync_Mode_supp	Yes
Supports automatic transmission rate detection	Auto_Baud_supp	Yes
PROFIBUS address modifiable by software	Set_Slave_Add_supp	No
Length of user-specific parameter assignment data	User_Prm_Data_Len	3 bytes
User-specific parameter assignment data	User_Prm_Data	Yes
Minimum interval between slave list rotations	Min_Slave_Intervall	1(100µs)
Modular device	Modular_Station	1

Feature	DP code word to IEC 61784-1:2002 Ed1 CP 3/1	BM 147 CPU
Maximum number of modules	Max_Module	35
Maximum number of inputs in bytes	Max_Input_Len	32
Maximum number of outputs in bytes	Max_Output_Len	32
Maximum combined number of inputs and outputs in bytes	Max_Data_Len	64
Central display of vendor-specific status and error messages	Unit_Diag_Bit	With LEDs “ON” and ”24 VDC”
Allocation of values in the station diagnostic field to texts	Unit_Diag_Area	Unassigned
Identifiers of all address areas for PROFIBUS	Module, End_Module	Yes
Allocation of vendor-specific error types in channel-specific diagnostic field to texts	Channel_Diag	No
Maximum length of the diagnostic data	Max_Diag_Data_Len	39 bytes

7.2 The mode selector and LEDs

Mode selector

The mode selector of the BM 147 CPU is located behind the front panel. It is designed as a 3-step toggle switch as shown below:

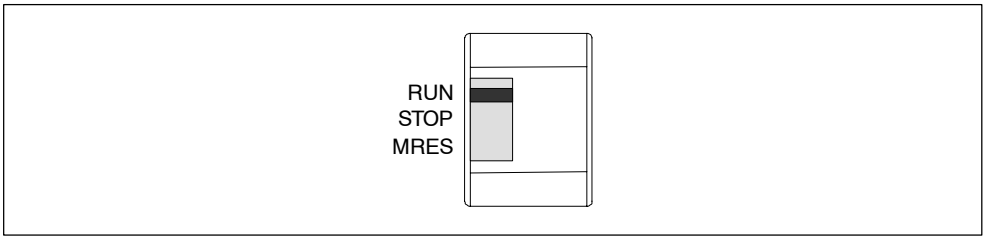


Figure 7-1 Mode selector

Positions of the mode selector

The positions of the mode selector are explained in the order in which they are arranged on the BM 147 CPU.

Table 7-1 Positions of the mode selector

Position	Description	Description
RUN	RUN mode	The CPU processes the user program.
STOP	STOP mode	The CPU processes no user program. Programs can: • Be read out from the CPU using a PD (CPU → PD) • Transferred to the CPU (PD → CPU)
MRES	Reset CPU memory	Momentary-contact position of the mode selector for resetting the CPU memory. You must adhere to a specific sequence when resetting the CPU memory using the mode selector (see Section 6.2)

Meanings of the LEDs for CPU functionality

For the BM 147 CPU there are 2 separate LEDs, which indicate the operating mode of the CPU:

- RUN
- STOP

You can obtain information on the power supply of the CPU, on force requests and on general errors via 3 additional LEDs.

Table 7-2 LEDs for CPU functionality

LED	Description	Description
ON (green)	Power on	**Comes on** when the supply voltage is applied to the CPU
RUN (green)	RUN mode	**Shines continuously** when the CPU is not processing the user program. **Flashes at 2 Hz** during CPU start-up: • For at least 3 secs, but the CPU start-up can also be shorter. • During the CPU start-up the STOP LED also lights up; when the STOP LED goes off, the outputs are enabled. **Flashes at 0.5 Hz** when the CPU has reached a breakpoint you have set. At the same time the STOP LED comes on.
STOP (yellow)	STOP mode	**Comes on** when the CPU • is not processing a user program. • Has reached a breakpoint you have set At the same time the RUN LED flashes at 0.5 Hz **Flashes** at 0.5Hz, when the CPU requests a memory reset (see Section 6.2).
FRCE (yellow)	Force request active	**Lights up** when a force request is active.
SF (red)	Group error	**Lights up** in the event of • Programming errors • Parameter assignment errors • Calculation errors • Timing errors • I/O errors • Hardware errors • Firmware errors To determine the exact nature of the error/fault, you have to use a PD and read out the contents of the diagnostic buffer.

Meanings of other LEDs

The “SF” (from the PROFIBUS-DP point of view), “BF-S”, “BF-M”, “ON” and “24 VDC” LEDs are described in Chapter 6.4.

7.3 SIMATIC Micro Memory Card

Micro Memory Card

A SIMATIC Micro Memory Card (MMC) is used as a memory module for the BM 147 CPU. The MMC can be used as a load memory and portable data carrier. It is an essential requirement for operating the BM 147 CPU. The following data is stored on the MMC:

- User program (all blocks)
- Archives and recipes
- Configuration data (*STEP 7* projects)
- Data for an operating system update, operating system backup

Note

On **one** MMC you can store **either** user and configuration data or the operating system.

Copy protection

The MMC has an internal serial number for the purpose of providing MMC copy protection at the user level. You can read out this serial number from the SZL parts list, $011C_H$ Index 8, using the SFC 51 RDSYSST.

For example, you can program a STOP command in a know-how protected block for the event that the set and actual serial number of the MMC do not match.

More detailed information can be found in the *SZL parts list in the instructions list* or in the *System and Standard Functions* manual.

Features

The SIMATIC micro memory card ensures zero maintenance and retentivity for the BM 147 CPU. More detailed information can be found in Section 7.4.

Caution

The module content of a SIMATIC micro memory card can be corrupted if the card is removed while a write operation is being performed. The MMC must then be erased at the PD or formatted in the BM 147 CPU.

Never remove the MMC in RUN mode; it should only be removed when the BM 147 CPU is in the POWER OFF or STOP mode and only if the PD is not currently performing a write access operation. If in the STOP mode you are not sure whether or not the PD is currently performing a write access operation (e.g. loading/erasing a block), unplug the communication connections beforehand.

Service life of an MMC

The service life of an MMC mainly depends on the following factors:

1. The number of erasing and programming operations
2. External influences such as the ambient temperature

At an ambient temperature of up to 60 °C, the service life of an MMC with max. 100,000 erase/write operations is 10 years.

Caution

To prevent data loss, never exceed the maximum number of erase/write operations.

Compatible SIMATIC Micro Memory Cards

The following memory modules are available:

Table 7-3 Available MMCs

Type	Order numbers
MMC 64k	6ES7 953-8LF00-0AA0
MMC 128k	6ES7 953-8LG00-0AA0
MMC 512k	6ES7 953-8LJ00-0AA0
MMC 2M	6ES7 953-8LL00-0AA0
MMC 4M	6ES7 953-8LM00-0AA0
MMC 8M	6ES7 953-8LP10-0AA0

The MMCs with a 4 MByte and 8 MByte memory are required for a firmware update.

Formatting the MMC prior to a memory reset

In the following exceptional cases, you have to format the MMC:

- The module type is not a user module.
- The MMC has not been formatted yet.
- The MMC is faulty.
- The content of the MMC is invalid.

The content of the MMC is designated as invalid, if

- the *Load User Program* operation has been interrupted by POWER OFF.
- the *Promming* operation has been interrupted by POWER OFF.
- a fault occurs during evaluation of the module content prior to a memory reset.
- a fault occurs during formatting, or formatting could not be performed.

If one of the above-described faults has occurred, the CPU also requests another memory reset after a memory reset has been performed. The content of the card is retained until the formatting has been completed, unless the Load User Program or Promming operations are interrupted by POWER OFF.

Format the MMC as follows:

When the BM 147 CPU requests a memory reset (the STOP LED flashes slowly), format it by operating the selector switch as follows:

1. Set the selector switch to the MRES position and hold it there (approx. 9 seconds) until the STOP LED remains lit (stops flashing).
2. Within the next 3 seconds you must release the selector switch and move it back to the MRES position. The STOP LED flashes during the formatting procedure.

Make sure that you perform the steps in the specified time, otherwise the MMC will not be formatted and will reassume the Memory Reset status.

The MMC is only formatted if a formatting condition (see above) exists and not e.g. when a memory reset is requested after a module is changed. In this case, switching to MRES only results in a standard memory reset whereby the content of the module remains valid.

Inserting/changing the card

The MMC is designed so that it can also be removed and inserted when the power is on. The BM 147 CPU must, however, be switched to the STOP mode (see the warning on page 7-7). The chamfered edge of the MMC prevents the card being inserted the wrong way round (reverse polarity protection).

The module slot and the mode selector are located behind the front panel on the BM 147 CPU. You can gain access to both elements by undoing the screws on the front panel and opening the panel.

There is an eject button on the memory card slot to enable you to remove the card easily. To eject the card, press the eject button with a small screwdriver or a ball-point pen.

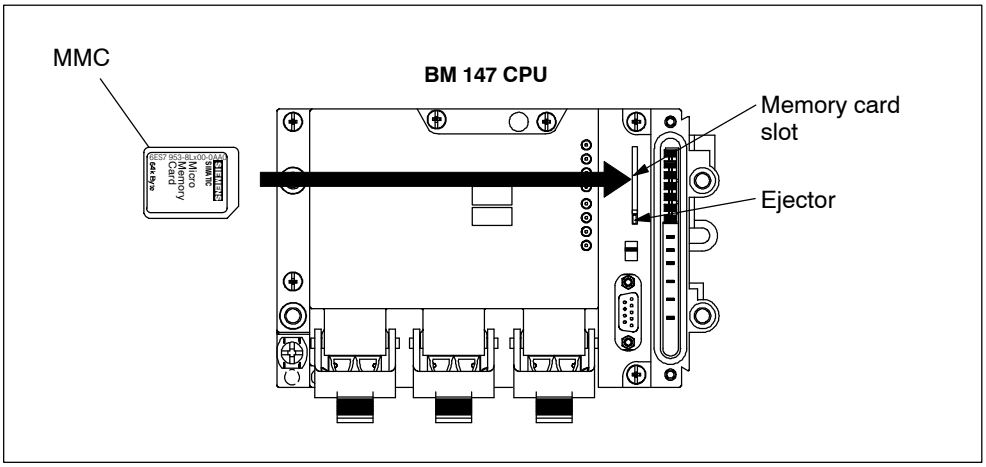


Figure 7-2 Position of the memory card slot for the MMC on the BM 147 CPU

If a new MMC is inserted in the memory card slot, the BM 147 CPU requests a memory reset.

Firmware update with MMC

To update the firmware, proceed as follows:

Table 7-4 Firmware update with MMC

Step	Action required	Action by the BM 147 CPU:
1.	Transfer update files to a blank MMC using *STEP 7* and your programming device ($\geq$ 4 MB).	-
2.	Deenergize the BM 147 CPU and insert the MMC with the FW update.	-
3.	Switch the power on	The BM 147 CPU automatically detects the MMC with the FW update and starts the FW update. All LEDs light up during the FW update. The STOP LED flashes after the FW update has been completed. In this way, the BM 147 CPU requests a memory reset.
4.	Deenergize the BM 147 CPU and unplug the MMC with the FW update.	-
5.	Switch on the power supply again.	The BM 147 CPU performs an automatic memory reset and is then ready for operation.

Backing up the operating system on the MMC

To back up the operating system, proceed as follows:

Table 7-5 Backing up the operating system

Step	Action required	Action by the BM 147 CPU:
1.	Insert a new micro memory card (≥ 4 MB) in the CPU	The CPU requests a memory reset
2.	Hold the mode selector in the MRES position.	–
3.	Switch the power off then on, and keep the mode selector in the MRES position until...	... STOP, RUN and FRCE LEDs start flashing
4.	Move the mode selector to STOP	–
5.	Move the mode selector briefly to MRES, then let it snap back to STOP	The BM 147 CPU starts to back up the operating system on the MMC. All the LEDs light up during backup. The STOP LED flashes after the backup has been completed. In this way, the BM 147 CPU requests a memory reset.
6.	Remove the micro memory card	–

7.4 Memory concept

7.4.1 Memory areas of the BM 147 CPU

Organization

The memory of the BM 147 CPU can be divided into three areas:

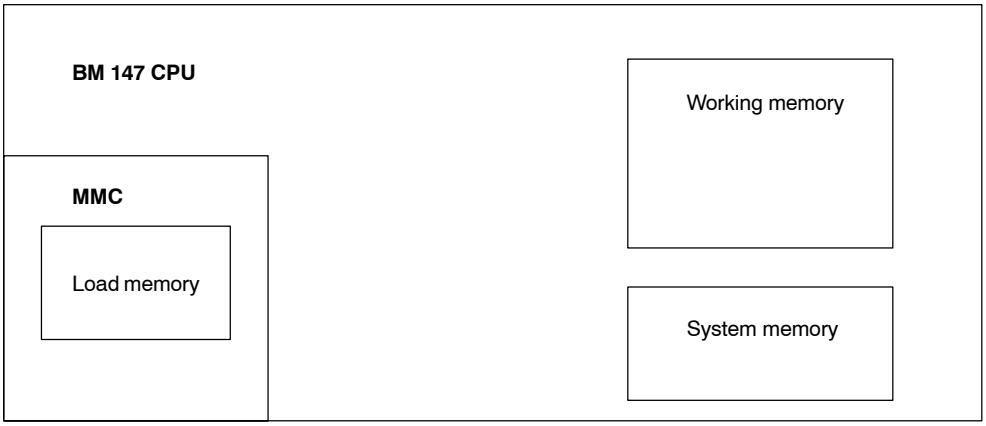


Figure 7-3 Memory areas of the BM 147 CPU

Load memory

The load memory is installed on a SIMATIC micro memory card (MMC). It is used to record code and data blocks as well as system data (configuration, connections, module parameters, etc.).

Blocks which are designated as non-process-related are recorded in the load memory.

The complete configuration data for a project can also be stored on the MMC.

Your program in the load memory (MMC) is always retentive. When downloaded, it is stored on the MMC such that it is unaffected by power failures and is not erased by memory resets.

Note

The BM 147 CPU can only be operated **with the MMC inserted**.

Working memory

The working memory is integrated on the CPU and cannot be expanded. It is used to process the codes and data of the user program. Program processing is only performed at the working memory and system memory.

The working memory of the CPU is retentive if the MMC is inserted.

Your data in the working memory is saved on the MMC if the power supply is interrupted.

System memory

The system memory is integrated on the CPU and cannot be expanded.

It contains

- the address areas ”memory markers”, ”timers” and ”counters”
- the process images of the inputs and outputs
- the local data

For memory markers, timers and counters, you can configure (Properties of the CPU, Retentivity tab) which parts are to be retentive and which parts are to be initialized with ”0” when a complete restart (warm restart) is performed.

The diagnostic buffer, MPI address (and transmission rate) as well as the run-time meter are generally stored in the retentive memory area on the CPU. Retentivity of the MPI address and transmission rate ensures that your CPU is still able to communicate following a power failure, a memory reset or the loss of communication parameters (by removing the MMC or erasing the communication parameters).

Retentivity

The BM 147 CPU has a retentive memory. The retentivity is provided on the MMC and CPU.

The retentivity means that the content of the retentive memory is retained even following POWER OFF and a restart (warm restart).

Retentive behavior of the memory objects

The following table shows the retentive behavior of the memory objects during the individual operating mode transitions.

Table 7-6 Retentive behavior of the memory objects

Memory object	Operating mode transition		
	POWER OFF/ POWER ON	STOP → RUN	Memory reset
User program/data (load memory)	X	X	X
Current values of the DBs	Can be set in the DB properties using *STEP 7* V5.2 + SP1 (see below)		–
Memory markers, timers and counters configured as retentive	X	X	–
Diagnostic buffers, run-time meters	X	X	X
MPI address, transmission rate	X	X	X

x = retentive; – = not retentive

Retentive behavior of a DB in BM 147 CPU

For BM 147 CPU, you can use *STEP 7* (as of version 5.2 + SP1) or the SFC 82 “CREA_DBL” (Parameter ATTRIB → Bit NON_RETAIN) to set whether, for POWER OFF/ON or STOP → RUN, a DB is to

- retain the current values (retentive DB) or
- adopt the initial values from the load memory (non-retentive DB).

Table 7-7 Retentive behavior of the DBs in BM 147 CPU

In the event of a POWER OFF/ON or a CPU restart, the DB is to	
Receive the initial values (non-retentive DB)	**Retain the last current values (retentive DB)**
Background: In the event of a POWER OFF/ON or a CPU restart (STOP → RUN), the current values of the DB are not retentive. The DB receives the initial values from the load memory.	Background: In the event of a POWER OFF/ON or a CPU restart (STOP → RUN), the current values of the DB are retained.
Prerequisite in *STEP 7*: • The “Non-Retain” checkbox is activated in the block properties of the DB or • A non-retentive DB was generated with the SFC 82 “CREA_DBL” and the associated block attribute (ATTRIB → Bit NON_RETAIN).	Prerequisite in *STEP 7*: • The “Non-Retain” checkbox is not activated in the block properties of the DB or • A retentive DB was generated with the SFC 82.

7.4.2 Memory functions

Introduction

You use the memory functions to generate, modify or erase user programs and individual blocks. The memory functions also allow you to archive your own project data in order to ensure the retentivity of your data.

General: Downloading the user program using the PD/PC

The complete user program is downloaded **to the BM 147 CPU from the MMC using the PD/PC**. In certain situations, all of the blocks stored in the load memory may be erased when the user program is downloaded.

In the load memory, blocks occupy the space specified under ”Load Memory Requirement” in the ”General Block Properties”.

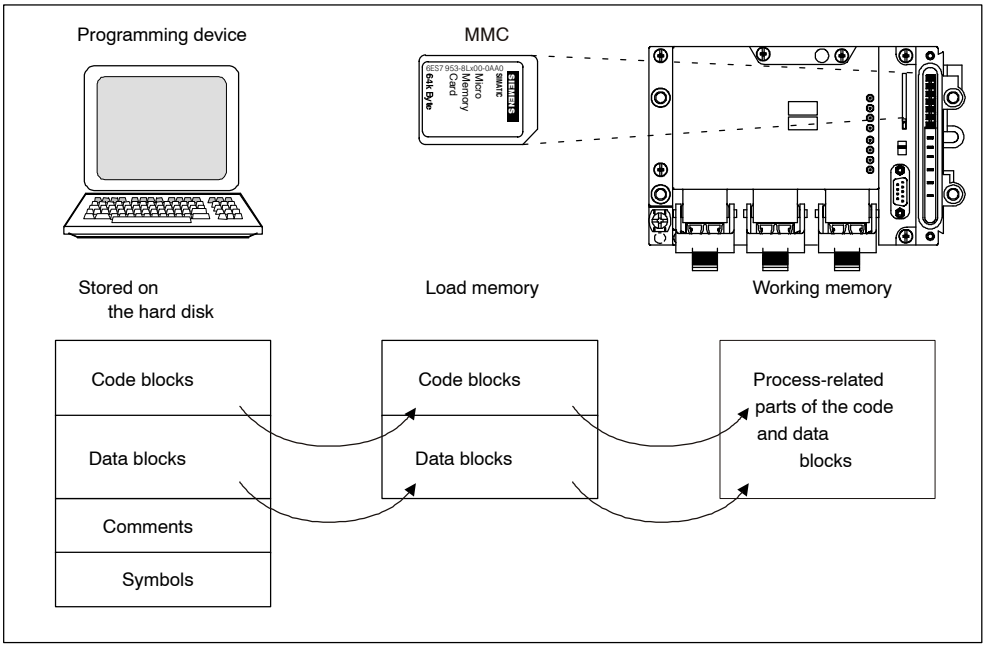


Figure 7-4 Load and working memory

The program cannot be started until all of the blocks have been loaded.

Note

The function is only permitted when the CPU is in STOP mode.

The load memory remains empty if loading could not be completed owing to a power failure or invalid blocks.

Downloading a user program to the MMC using the PD/PC

Case A: Downloading a new user program
You have created a new user program. Download the complete program to the MMC using the PD/PC.

Case B: Reloading blocks
You have already created a user program and downloaded it to the MMC (case A). You can then add further blocks to the user program. To do so, you do not have to download the complete user program to the MMC again; you only have to reload the new blocks to the MMC (this method shortens the loading time in the case of very complex programs!).

Case C: Overloading
In this case, you make changes to blocks of your user program. You then overload the user program or only the modified blocks to the MMC using the PD/PC.

Warning

When blocks/a user program are overloaded, all of the data stored on the MMC under the same name is lost.

When a block has been downloaded, the content in the case of process-related blocks is transferred to the working memory and activated.

Erasing blocks

When a block is erased, it is deleted from the load memory. It is possible to erase data blocks from the user program (SFC 23 ”DEL_DB”).

If memory in the working memory has been occupied by this block, this memory is released.

Uploading

Unlike downloading, uploading involves loading individual blocks or a complete user program **from the CPU to the PD/PC**. In this case, the blocks have the same content as when last downloaded to the MMC. Process-related data blocks are the exception; they receive the current values.

Uploading blocks or the user program from the CPU using *STEP 7* does not have any effect on the memory assignment of the CPU.

Compression

Compression fills any gaps between memory objects which are formed by loading and erasing operations in the load and working memory. Contiguous areas of free memory are then available.

Compression is possible when the CPU is in both the STOP and RUN mode.

Promming (RAM to ROM)

With promming, the current values of the data blocks are transferred from the working memory to the load memory where they serve as new initial values for the DB.

Note

The function is only permitted when the CPU is in STOP mode.

The load memory remains empty if the function could not be completed owing to a power failure.

Removing/inserting the MMC

The BM 147 CPU cannot run if there is no MMC inserted in the BM 147 CPU (no load memory available). Practical operation is only possible if an MMC has been inserted and a memory reset has been performed.

Removal and insertion of an MMC is detected by the BM 147 CPU in all operating modes.

Removing:

1. The BM 147 CPU must be in the STOP mode.
2. The PD must not be performing any write access operations (e.g. loading blocks)
3. When the MMC is removed, the BM 147 CPU requests a memory reset

Caution

The module content of a SIMATIC micro memory card can be corrupted if the card is removed while a write operation is being performed. The MMC must then be erased at the PD or formatted in the BM 147 CPU.

Never remove the MMC in RUN mode; it should only be removed when the BM 147 CPU is in the POWER OFF or STOP mode and only if the PD is not currently performing a write access operation. If in the STOP mode you are not sure whether or not the PD is currently performing a write access operation (e.g. loading/erasing a block), unplug the communication connections beforehand.

Inserting:

The MMC with the appropriate user program is inserted as follows:

1. Insert the MMC
2. The BM 147 CPU requests a memory reset
3. Acknowledge the memory reset

   If the BM 147 CPU requests a memory reset again owing to an incorrect MMC or an MMC with a firmware update being inserted, proceed as described in Section 7.3 under *Special measure*.
4. Start the BM 147 CPU

Warning

Make sure that the MMC to be inserted contains the user program appropriate for the BM 147 CPU (for the system). An incorrect user program can have serious effects on processing.

Memory reset

A memory reset restores defined conditions following removal/insertion of the micro memory card so that the BM 147 CPU can be restarted (warm restart).

When the memory is reset, the memory administration system of the BM 147 CPU is reorganized. All blocks of the load memory are retained. All process-related blocks are transferred again from the load memory to the working memory; this initializes the data blocks in the working memory (they receive their initial values from the load memory again).

The memory reset procedure and the special points associated with it are described in Section 6.2.

Restart (warm restart)

- All DBs retain their current values.
- All retentive Ms, Cs and Ts retain their values.
- All non-retentive user data is initialized:
  - M, C, T, I, O with ”0”
- All processing levels start from the beginning.
- The process images are erased.

7.4.3 Address areas

Overview

The system memory of the BM 147 CPU id divided into address areas (see the table below). In your program, you use the appropriate operations to address the data directly in the respective address area.

Table 7-8 Address areas of the system memory

Address area	Description
Process image of the inputs	At the beginning of each OB 1 cycle, the BM 147 CPU reads the inputs out of the input modules and stores the values in the process image of the inputs.
Process image of the outputs	During the cycle, the program calculates the values for the outputs and stores them in the process image of the outputs. At the end of the OB 1 cycle, the BM 147 CPU writes the calculated output values to the output modules.
Memory markers	This area provides memory for intermediate results calculated in the program.
Timers	Timers are available in this area.
Counter	Counters are available in this area.
Local data	This memory area records the temporary data of a code block (OB, FB, FC) during the period in which this block is being processed.
Data blocks	See Section 7.4.4

The *Instruction list* tells you which address areas are possible with your CPU.

Process image of the inputs and outputs

If the address areas ”inputs” (I) and ”outputs” (O) are addressed in the user program, the signal states on the digital expansion modules are not checked, but instead a memory area in the system memory of the CPU is accessed. This memory area is referred to as the process image.

The process image is divided into two parts: the process image of the inputs and the process image of the outputs.

Advantages of the process image

The advantage of accessing the process image over accessing the expansion modules directly is that a consistent image of the process signals is available to the CPU for the duration of cyclic program processing. If a signal state at an input module changes during program processing, the signal state is retained in the process image until the process image is updated in the next cycle. Furthermore, accessing the process image requires much less time than accessing the expansion modules directly because the process image is located in the system memory of the CPU.

Updating the process image

The process image is updated by the operating system cyclically. The figure below shows the processing steps within a cycle.

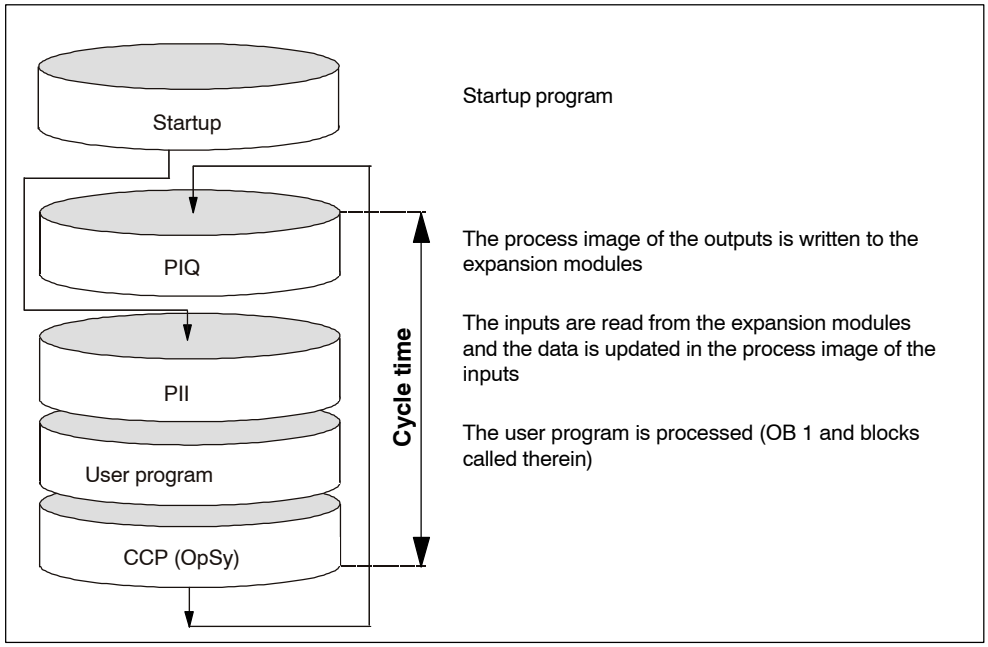


Figure 7-5 Processing steps within a cycle

Local data

The following are stored as local data:

- The temporary variables of code blocks
- The start information of the organization blocks
- Transfer parameters
- Intermediate results

Temporary variables

When creating blocks, you can declare temporary variables (TEMP) which are only available while the block is being processed and are then overwritten again. This local data has a fixed length for each OB. The local data must be initialized before the first read access operation. Furthermore, each organization block requires 20 bytes for its start information. Local data is accessed faster than data in the DBs.

The BM 147 CPU has memory for the temporary variables (local data) of blocks that have just been processed. This memory is divided equally between the priority classes. Each priority class has its own local data area.

Caution

All temporary variables (TEMP) of an OB and its subordinate blocks are stored in the local data. The local data area could overflow if you use a large number of nesting levels for block processing.
The BM 147 CPU changes to the STOP mode if you exceed the permitted quantity of local data in a priority class.
Take into consideration the amount of local data required by the synchronous fault OBs. In each case, the local data requirement is assigned to the responsible priority class.

7.4.4 Handling data in DBs

Recipes

A recipe is a collection of user data.

A simple recipe concept can be realized using non-process-related data blocks. The recipes should have the same structure (length). There should be one DB for each recipe.

Processing sequence of a recipe

The recipe is to be stored in the load memory:

- The individual data records of the recipes are created as non-process-related DBs using *STEP 7* and downloaded to the BM 147 CPU. The recipes therefore only occupy space in the load memory and not in the working memory.

Working with the recipe data:

- Calling the SFC 83 ”READ_DBL” from the user program causes the data record of the current recipe to be read out of the DB in the load memory and into a process-related DB in the working memory. As a result, the working memory only has to accommodate the data from one data record.

  The user program can now access the data of the current recipe.

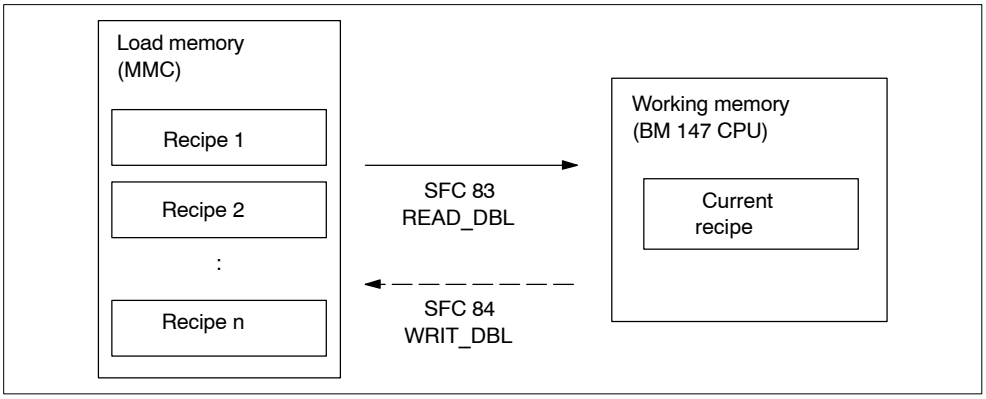


Figure 7-6 Handling recipe data

Writing back a modified recipe:

- Calling the SFC 84 ”WRIT_DBL” from the user program writes new or modified data records of a recipe, which are created during program processing, back to the load memory.

  The data written to the load memory is not erased by a memory reset and is transferrable.

  If modified data records (recipes) are to be stored on the PD/PC, they can be uploaded and stored there as a complete block.

Measured value archives

Measured values are created when the user program is processed by the BM 147 CPU. These measured values are to be archived and evaluated.

Processing sequence of a measured value archive

Collecting the measured values:

- The measured values in the working memory are collected in a DB (for alternating buffer operation in several DBs) by the BM 147 CPU.

Archiving the measured values:

- Calling the SFC 84 ”WRIT_DBL” from the user program moves the measured values in the DB to the load memory before the data volume can exceed the memory capacity of the working memory.

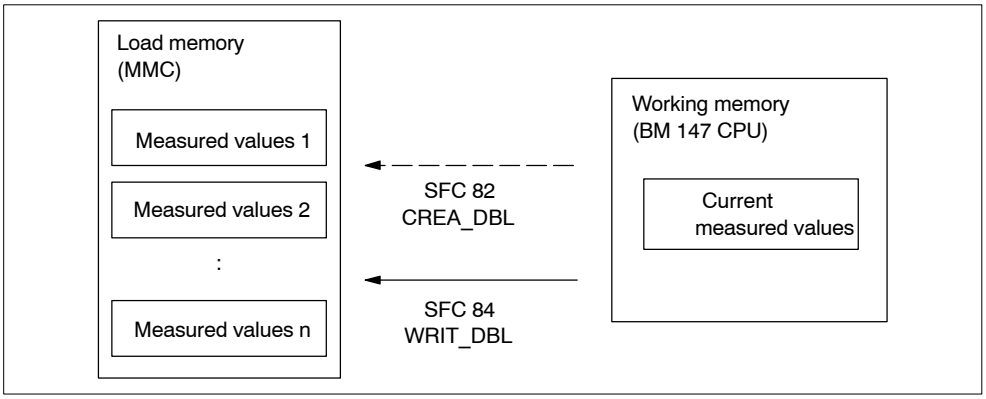


Figure 7-7 Handling measured value archives

- Calling the SFC 82 ”CREA_DBL” from the user program generates new (additional) DBs as non-process-related DBs in the load memory. These non-process-related DBs do not require space in the working memory.

Note

If a DB with the same name already exists in the load memory and/or working memory, the SFC 82 is terminated and an error display is generated.

The data written to the load memory is not erased by a memory reset and is transferrable.

Evaluating the measured values:

- The measured value data blocks stored in the load memory can be uploaded and evaluated by other communication partners (e.g. PD, PC, ...).

MMC access

Note

Active system functions SFC 82 to 84 (current access to the MMC) have a major influence on PD functions (e.g. status block, status variable, download block, upload block, open block). Their performance is typically 10 times lower (compared to non-active system functions).

To prevent data loss, never exceed the maximum number of erase/write operations of an MMC. Refer also to Section 7.3.

Caution

The module content of a SIMATIC micro memory card can be corrupted if the card is removed while a write operation is being performed. The MMC must then be erased at the PD or formatted in the CPU.

Never remove the MMC in RUN mode; it should only be removed when the CPU is in the POWER OFF or STOP mode and only if the PD is not currently performing a write access operation. If in the STOP mode you are not sure whether or not the PD is currently performing a write access operation (e.g. loading/erasing a block), unplug the communication connections beforehand.

7.4.5 Storing/download entire projects on/from Micro Memory Cards

You will find a detailed description of these functions in the *Online Help for STEP 7*.

7.5 Interface

The **BM 147-1 CPU** has a coexistent MPI/DP interface that is physically available on several connectors.

- The MPI interface is available at the 9-pin Sub-D connector, X03 (MPI), under the front panel.
- The PROFIBUS-DP interface is available at the ECOFAST connectors, X01 (DP-IN) and X02 (DP-OUT).

In addition to the coexistent MPI/DP interface, the **BM 147-2 CPU** (as for the BM 147-1 CPU) also has a PROFIBUS-DP master interface, X04 (DP-M).

The interfaces are described below.

MPI interface

The MPI (Multi Point Interface) is the interface of the BM 147 CPU to a PD/OP and the interface allowing communication in an MPI network. The BM 147 CPU has an **MPI interface** which functions with RS 485.

The typical (default) transmission rate is 187.5 kbaud. The BM 147 CPU supports all MPI transmission rates.

The BM 147 CPU automatically sends the set bus parameters (e.g. the transmission rate) to the MPI interface. A programming device, for example, is thus supplied with the correct parameters and can automatically connect to an MPI subnetwork.

Note

- You can only connect PDs to the MPI subnetwork during operation.
  Other nodes (e.g. OP, TP, ...) should not be connected to the MPI subnetwork during operation, otherwise the transmitted data could be corrupted by interference noises or global data packets could be lost.
- Note that 24 volts are not available at the MPI interface (9-pin Sub-D connector) (see also Table 9-1).
  You cannot operate nodes on the X03 that are only supplied with 24 volts via the 9-pin Sub-D connector.

PROFIBUS-DP interface

The PROFIBUS-DP interface is mainly used to connect distributed I/Os. You use the PROFIBUS-DP to configure extended subnetworks. Transmission rates of up to 12 Mbaud are possible on the PROFIBUS.

The BM 147 CPU has a **PROFIBUS-DP interface**. This can be configured to be active or passive.

The BM 147 CPU as active station sends the set bus parameters (e.g. the transmission rate) to the PROFIBUS-DP interface. A programming device, for example, is thus supplied with the correct parameters and can automatically connect to a PROFIBUS subnetwork. The sending of bus parameters can be deactivated in the configuration settings.

DP master interface

The DP master interface on the BM 147-2 CPU is used to connect the distributed I/O (slaves). Transmission rates of up to 12 Mbaud are possible.

The DP master interface can be configured to be a DP master or to be inactive.

- As a DP master the interface requires a configuration. Slaves can be operated when the configuration is loaded; PD/OP functions and routing are possible.
- The interface is always inactive when there is not configuration.

Which devices can be connected to which interface?

Table 7-9 Connectable devices

MPI [1)]	PROFIBUS-DP (DP-IN/DP-OUT)	DP master interface (DP-M)
• PD/PC • OP/TP • S7-300/400 with MPI interface • S7-200 (only with 19.2 kbaud)	• DP master • Actuators/sensors • S7-300/400 with PROFIBUS-DP interface • PD/PC • OP/TP	• DP slaves • Actuators/sensors • S7-300/400 with PROFIBUS-DP interface • PD/PC • OP/TP

1) 24 V are not available, see note in Section “MPI interface”

Further information

More detailed information on the individual connections can be found in the *Communication with SIMATIC* manual.

7.6 Clock

The BM 147 CPU has an integrated hardware clock.

Setting, reading and programming the clock

You set and read the clock using the programming device (see the *STEP 7*) User Manual) or program the clock in the user program using SFCs (see the *System and Standard Functions* Reference Manual and *Instruction list*)).

Features

The table below indicates the features and functions of the clock.

When you parameterize the CPU in *STEP 7*, you can also set functions such as synchronization via the MPI interface and correction factors (refer to the *STEP 7* online help for information on how to do this).

Table 7-10 Features of the clock

Features	BM 147 CPU
Type	Hardware clock
Manufacturer setting	DT#1994-01-01-00:00:00
Backup	By means of integrated capacitor
Backup time	Typ. 6 weeks (at ambient temperature of 40 °C)
Run-time meter	1

Behavior of the clock when power is off

The clock of the CPU continues to run after the power has been switched off.

When the backup time has expired, the clock begins to run at the time at which the power was switched off.

7.7 S7 connections

Introduction

If S7 modules communicate with each other, a so-called S7 connection is built up between the modules. This forms the communication route.

Note

Global data communication does not require S7 connections.

Each communication connection requires S7 connection resources on the CPU; these must exist for the duration of the specific connection.

Therefore, a specific number of S7 connection resources is made available on each S7 CPU that are used by different communication utilities (PD/OP communication, S7 communication or S7 basic communication).

What are S7 connection points?

The S7 connection between communications-capable modules is established between connection points. Therefore, the S7 connection always has two connection points: an active and a passive connection point.

- The active connection point is assigned to the module that builds up the S7 connection.
- The passive connection point is assigned to the module that accepts the S7 connection.

Each communications-capable module can become a connection point of an S7 connection. At the connection point, the established communication connection always occupies **one** S7 connection of the specific module.

Pass-through point of an S7 connection

If you use the routing functionality, the S7 connection between two communications-capable modules is built up over several subnetworks. These subnetworks are connected to each other through a gateway. The module that is used to implement this gateway is called the router. Thus, the router is the pass-through point of an S7 connection.

Each BM 147-2 CPU can be the router of an S7 connection. The BM 147-2 CPU can build up a maximum of 4 routing connections that do not restrict the quantity structure of the S7 connections.

Assigning S7 connections

The S7 connections on a communications-capable module can be assigned in various ways:

Reserving connections during configuration

- If, in *STEP 7*, a CPU is plugged in when the hardware is configured, S7 connections are automatically reserved on this CPU for both the PD and OP communication.
- For PD and OP communication and for S7 basic communication, the S7 connections can be reserved in *STEP 7*.

Assigning connections by programming

For the S7 basic communication, the connection is established via the user program. The CPU operating system initiates the build up of the connection and the corresponding S7 connections are assigned.

Assigning connections upon commissioning, testing and diagnosis

S7 connections for the PD communication are assigned by means of an online function on the Engineering Station (PD/PC with *STEP 7*):

- If an S7 connection was reserved in the CPU for PD communication when the hardware was configured, it is allocated to the Engineering Station, i.e. it is simply assigned.
- If all reserved S7 connections for PD communication have already been assigned and unreserved S7 connections are still fee, the operating system allocates a connection that is still free. If there are no longer any free connections, the Engineering Station cannot communicate online with the CPU.

Assigning connections for B&B utilities

S7 connections for the OP communication are assigned by means of an online function on the B&B Station (OP/TP/... with *ProTool*) :

- If an S7 connection was reserved in the CPU for OP communication when the hardware was configured, it is allocated to the B&B Station, i.e. it is simply assigned.
- If all reserved S7 connections for OP communication have already been assigned and unreserved S7 connections are still fee, the operating system allocates a connection that is still free. If there are no longer any free connections, the B&B Station cannot communicate online with the CPU.

Sequence of the assignment of S7 connections

When the system is configured with *STEP 7*, parameter blocks are generated that are read out when the module is initialized. Thus, the module operating system reserves or assigns the corresponding S7 connections. This means, for example, that an Operator Station cannot access a reserved S7 connection for PD communication.

If the module (CPU) also has S7 connections that are not reserved, these are free to be used as required. The assignment of these S7 connections is in the order in which the requirements arises.

Example

If there is only one remaining free S7 connection on the CPU, you can connect a PD to the bus. The PD is then able to communicate with the CPU. However, the S7 connection is only assigned when the PD communicates with the CPU.

If you connect an OP to the bus at precisely the time when the PD is not communicating, the OP builds up a connection to the CPU. However, because an OP, unlike a PD, maintains a permanent communication connection, you will no longer be able to establish a connection via the PD.

Distribution of the S7 connections

The distribution of the S7 connections of the CPUs are shown in the table below:

Table 7-11 Distribution of the S7 connections

Communication utility	Distribution
PD communication OP communication S7 basic communication	So that the assignment of the S7 connections does not depend solely on the sequence in which the various communication utilities arise, S7 connections can be reserved for these utilities. For the PD and OP communication, at least one S7 connection is reserved for each as a preassignment. The table below and the technical data show the S7 connections that can be adjusted and the presettings for the BM 147 CPU. A “redistribution“ of the S7 connections is set up in *STEP 7* when the CPU is parameterized.
S7 communication Other communication connections (e. g. via CP 343-1 with data lengths > 240 byte)	The available S7 connections that have not been reserved for a specific utility (PD/OP communication, S7 basis communication) are assigned for this purpose.
Routing of PD functions (BM 147-2 CPU only)	The CPUs make available 4 connections for routing from PD functions. These connections are additional to the S7 connections.
Global data communication	This communication utility does **not** use S7 connections.

Availability of the S7 connections

The table below shows the S7 connections available on the BM 147 CPU.

Table 7-12 Availability of the S7 connections

Parameters	BM 147 CPU
Total number of S7 connections	12
• Reserved for PD communication	1 to 11 Default: 1
• Reserved for OP communication	1 to 11 Default: 1
• Reserved for S7 basic communication	0 to 10 Default: 0
• Free S7 connections	All unreserved S7 connections are shown as free connections.

Example for a BM 147 CPU

The BM 147 CPU makes 12 S7 connections available:

- Reserve 2 S7 connections for PD communication.
- Reserve 3 S7 connections for OP communication.
- Reserve 1 S7 connection for S7 basic communication.

There remain 6 S7 connections for other communication utilities, such as S7 communication, OP communication, etc.

More detailed information

- More detailed information on SFCs can be found in the *Instruction list*, in the *STEP 7 Online Help* or in the *System and Standard Functions* Reference Manual.
- More detailed information on communication can be found in the *Communication with SIMATIC* manual.
- More detailed information on routing can be found in Chapter 7.9 and in the *STEP 7 Online Help*.

7.8 Communication

Communication utilities of the BM 147 CPU

The selected communication utility influences

- the functionality available to the user
- whether or not an S7 connection is required
- the time at which the connection is set up

The user interface can be very different (SFC, SFB, ...) and also depends on the used hardware (SIMATIC-CPU, PC, ...).

The BM 147 CPU provides the following communication utilities:

Table 7-13 Communication utilities of the BM 147 CPU

Communication utility	Functionality	S7 connection	Via MPI	Via DP
PD communication	Commissioning, testing, diagnostics	Set up by the PD as soon as the utility is used	x	x
OP communication	Operating and monitoring	Set up by the OP when switched on	x	x
S7 basic communication	Data exchange	Programmed by means of blocks (parameters at SFC)	x	–
S7 communication	Data exchange	BM 147 CPU only as server; connection set up by the communication partner	x	x
Global data communication	Cyclic data exchange (e.g. memory markers)	Does not require an S7 connection	x	–
Routing of PD functions	For example, testing and diagnosis across network boundaries	Set up by the PD as soon as the utility is used	x	x

Chapters 3 and 4 contain information on network configuration and addressing.

PD communication

PD communication enables data exchange between engineering stations (e.g. PD, PC) and communications-capable SIMATIC modules. The utility is possible on MPI and PROFIBUS subnetworks. The transition between subnetworks is also supported.

PD communication provides functions which are required for downloading programs and configuration data, for executing tests and evaluating diagnostic information. These functions are integrated in the operating system of the SIMATIC S7 modules.

A CPU can maintain several online connections to one or more PDs simultaneously.

OP communication

OP communication enables data exchange between operator stations (e.g. OP, TP) and communications-capable SIMATIC modules. The utility is possible on MPI and PROFIBUS subnetworks.

OP communication provides functions which are required for operation and monitoring. These functions are integrated in the operating system of the SIMATIC S7 modules.

A CPU can maintain several connections to one or more OPs simultaneously.

S7 basic communication

S7 basic communication enables data exchange between S7-CPUs and communications-capable SIMATIC modules within an S7 station (acknowledged data exchange). Data is exchanged by means of non-configured S7 connections. The utility is possible on the MPI subnetwork or in the station of function modules (FM).

S7 basic communication provides functions which are required for data exchange. These functions are integrated in the operating system of the BM 147 CPU.

The user can use the utility via the ”System Function” user interface (SFC).

S7 communication

BM 147 CPU can only be a server in S7 communication. The connection is always set up by the communication partner. The utility is possible on MPI and PROFIBUS subnetworks.

The utilities are processed by the operating system without an explicit user interface.

Global data communication

Global data communication enables the cyclic exchange of global data (e.g. I, O, M) between SIMATIC S7-CPUs (unacknowledged data exchange). The data is sent to all CPUs in the MPI subnetwork simultaneously by the CPU. This function is integrated in the operating system of the BM 147 CPU.

Transmit and receive conditions

You should observe the following conditions for communication in GD circles:

- The following must apply for the sender of a GD packet:
  $\text{Scan rate}_{\text{Sender}} \times \text{Cycle time}_{\text{Sender}} \geq 60\ \text{ms}$
- The following must apply for the recipient of a GD packet:
  $\text{Scan rate}_{\text{Recipient}} \times \text{Cycle time}_{\text{Recipient}} < \text{Scan rate}_{\text{Sender}} \times \text{Cycle time}_{\text{Sender}}$

A GD packet could be lost if you do not observe these conditions. Reasons for this are:

- the performance of the ”smallest” CPU in the GD circle
- global data is sent and received asynchronously by the sender and recipient

If in *STEP 7* you set: ”Send After Each CPU Cycle” and the CPU has a short CPU cycle (< 60 ms), the operating system could then overwrite a GD packet on the CPU which has not yet been sent. The loss of global data is indicated in the status field of the GD circle, provided that you have configured this option with *STEP 7*.

Scan rate

The scan rate indicates how many cycles the GD communication is divided into. You can set the scan rate when configuring the global data communication in *STEP 7*. If, for example, you select a scan rate of 7, global data communication only occurs every 7 cycles. This relieves the load on the CPU.

GD resources

The table below shows the GD resources of the BM 147 CPU.

Table 7-14 GD resources of the BM 147 CPU

Parameters	BM 147 CPU
Number of GD circles per CPU	Max. 4
Number of transmit GD packets per GD circle	Max. 1
Number of transmit GD packets for all GD circles	Max. 4
Number of receive GD packets per GD circle	Max. 1
Number of receive GD packets for all GD circles	Max. 4
Data length per GD packet	Max. 22 bytes
Consistency	Max. 22 bytes
Scan rate (default)	1 to 255 (8)

Routing

By means of a BM 147-2 CPU configured as a master and with *STEP 7* as of V 5.2 + Service Pack 1, you can reach S7 stations across different subnetworks (MPI interface / PROFIBUS-DP interface) using a PD/PC.

For example, you can load user programs or a hardware configuration or perform testing and commissioning functions.

Note

If you use the BM 147-2 CPU as an Intelligent Slave, the routing function can only be used when the slave interface is active and the DP master interface has been parameterized.
To do so, activate the Commissioning/Test Mode checkbox in the DP interface properties in *STEP 7* (see Chap. 3.1).

Detailed information can be found in the *Programming with STEP 7* manual or directly in the *STEP 7 Online Help*.

More detailed information

- More detailed information on SFCs can be found in the *Instruction list*, in the *STEP 7 Online Help* or in the *System and Standard Functions* Reference Manual.
- More detailed information on communication can be found in the *Communication with SIMATIC* manual.

7.9 Routing

Access from a PD/PC to stations in another subnetwork

As of *STEP 7* V5.2 + Service Pack 1, you can reach S7 stations across subnetwork boundaries with the PD/PC, for example to load user programs or a hardware configuration or to perform testing and diagnosis functions.

The routing function lets you connect a PD anywhere in the network and establish a connection to any station that can be reached via the gateways.

The BM 147-2 CPU makes available 4 connections for routing PD functions. These connections are additional to the S7 connections.

Note

If you use the BM 147-2 CPU as an Intelligent Slave, the routing function can only be used when the slave interface is active and the DP master interface has been parameterized.
To do so, activate the Commissioning/Test Mode checkbox in the DP interface properties in *STEP 7* (see Chap. 3.1).

Detailed information can be found in the *Programming with STEP 7* manual or directly in the *STEP 7 Online Help*.

Gateway

The gateway from one subnetwork to one or more other subnetworks lies in a SIMATIC station that has interfaces to the respective subnetworks. Thus, in the diagram below, the CPU 31xC-2 DP acts as a router between subnetwork 1 and subnetwork 2.

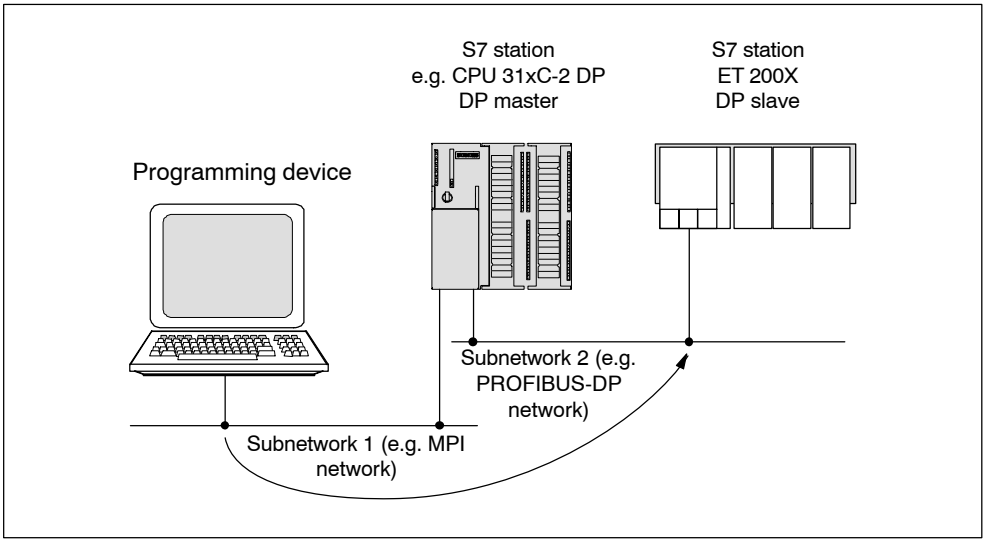


Figure 7-8 Routing gateway

Prerequisites

- The modules of the station are “capable of routing” (CPUs or CPs).
- The network configuration does not extend beyond the project boundaries.
- The modules have loaded in them the configuration information that contains the current “knowledge” on the entire network configuration of the project.

  Reason: All modules that participate in the gateway must contain information on which subnetworks can be reached along which routes (= routing information).
- The PD/PC with which you wish to establish a connection via a gateway must be assigned in the network configuration to the network to which it is actually physically connected.
- The CPU must be configured as a master.
- If the CPU is configured as a slave, the Commissioning/Test Mode functionality must be activated in the DP interface properties for the DP slave in *STEP 7*.

Application example: TeleService

As an application example, the following figure shows the teleservice of an S7 station by a PD. The connection is established across subnetwork boundaries and by means of a modem connection.

The lower section of the figure show how easily this can be configured in *STEP 7*.

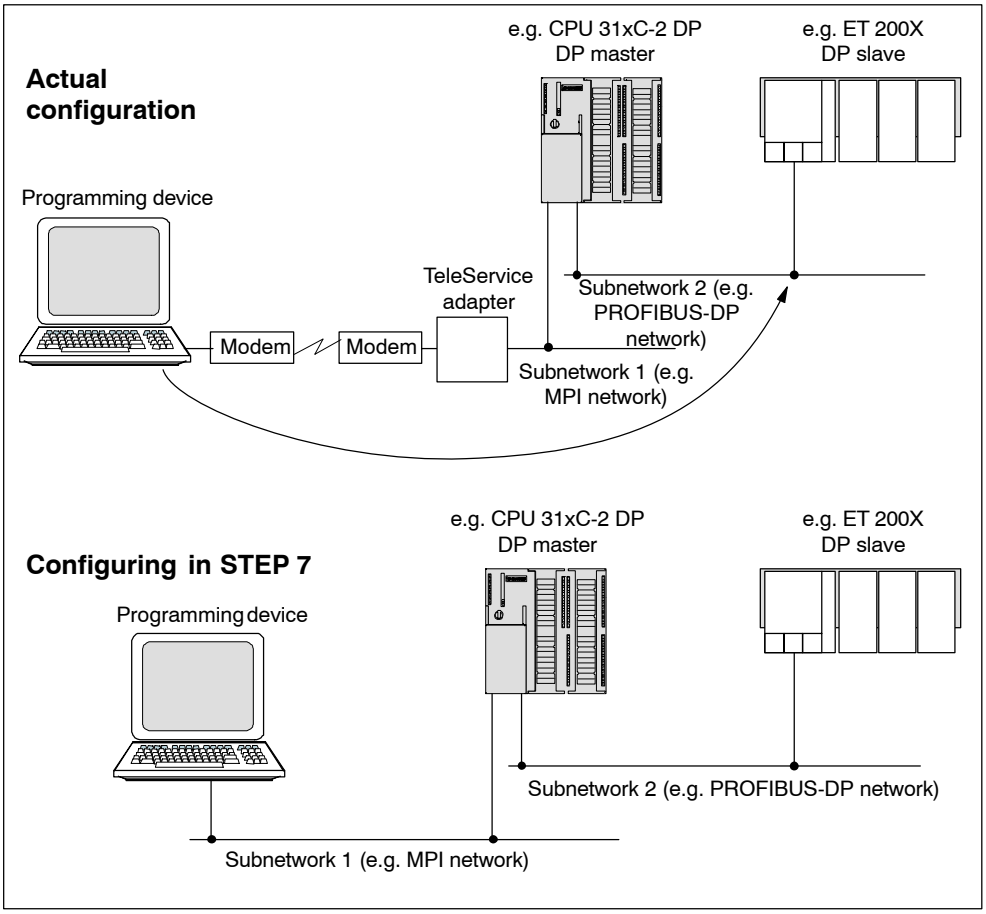


Figure 7-9 Routing – TeleService application example

More Information ...

- More information on the configuration using *STEP 7* can be found in the *Configuring hardware and connections with STEP 7* manual.
- More basic information can be found in the *Communication with SIMATIC* manual.
- More information on the TeleService adapter can be found in the Internet. In the Manual Search section, you can find the relevant documentation to download under the A5E00078070 search term.

7.10 Data consistency

A data area is said to be consistent if it can be read/written by the operating system as a single block. The data that is transmitted together between devices should stem from one processing cycle and thus should form a unit, i.e. be consistent.

If there is a programmed communication function in the user program, for example X-SEND/ X-RCV, that accesses shared data, the access to this data area itself can be coordinated using the “BUSY“ parameter.

For PUT/GET functions

For S7 communication functions, such as PUT/GET and read/write via OP communication, that do not require a block in the user program of the CPU (as server), the size of the data consistency must be taken into account during programming.

The PUT/GET functions of the S7 communication or reading/writing of variables via the OP communication are processed in the cycle checking point of the CPU.

To ensure a defined process alarm reaction time, the communication variables are consistently copied in blocks of a maximum of 64 bytes in the cycle checkpoint of the operating system into and out of the user memory or memories. Data consistency is not guaranteed for any large data areas.

If a defined data consistency is required, the communication variables in the user program of the CPU may not exceed 64 bytes in size.

7.11 Blocks

This section provides an overview of the blocks that will run in the BM 147 CPU.

The operating system is designed for event-driven processing of the user program. The following tables show which organization blocks (OBs) the operating system automatically invokes in response to which events.

More information

You will find a detailed description of the blocks in the *System and Standard Functions Reference Manual*. There is an overview of all the *STEP 7* documentation in the *ET 200X Distributed I/O System* manual.

Overview of all the blocks

Table 7-15 Overview of the Blocks

Block	Number	Area	Maximum size	Remarks
OB	13 (BM 147-1 CPU) 16 (BM 147-2 CPU)	–	16 kB	All the possible OBs are found in the *Instruction list*.
FC	512	0-511		–
FB	512	0-511		–
DB	511	1-511		0 is reserved
SFC	61	–	–	All SFCs for the CPU are found in the *Instruction list*.
SFB	11	–	–	All SFBs for the CPU are found in the *Instruction list*.

A maximum of 1024 blocks (number of FBs + FCs + DBs) can be loaded in each BM 147 CPU.

SFC 55 “WR_PARM”, SFC 56 “WR_DPARM”, SFC 57 “PARM_MOD”, SFC 58 “WR_REC”

The use of SFCs 55 to 58 in conjunction with your BM 147 CPU is not recommended owing to the static module parameters.

If you do use SFCs 55 to 58 in conjunction with your BM 147 CPU, the BM 147 CPU could malfunction.

Points to note about OB 122

Note

Note the following about OB 122:

The CPU enters the value ”0” in the following temporary variables of the variable declaration table in the local data of the OB:

- **Byte No. 3:** OB122_BLK_TYPE
  (type of block in which the error occurred)
- **Byte No. 8 and 9:** OB122_BLK_NUM
  (number of block in which the error occurred)
- **Byte No. 10 and 11:** OB122_PRG_ADDR
  (address of block in which the error occurred)

7.12 Parameters

Parameterizable features

The properties and responses of the BM 147 CPU can be parameterized. You carry out this parameterization on different tabs in *STEP 7*.

Which parameters can be set for the BM 147 CPU?

The following table contains all the parameter blocks for the BM 147 CPU. The parameters are explained in the *STEP 7 Online Help*.

Table 7-16 Parameter blocks, settable parameters and their ranges for the BM 147 CPU

Parameter blocks	Settable parameters	Range
Startup	Startup at preset configuration not equal to actual configuration	Yes/no
	Startup after power on	Warm restart
	Monitoring time for: • "Finished" message by means of modules (100 ms) • Transfer of the parameters to modules (100 ms)	 1 to 650 1 to 10000
Diagnostics/Clock	Report cause of STOP	Yes/no
	Synchronization in PLC • Type • Interval	 None/as master 1 s/10 s/1 min/10 min/1 h/12 h/24 h
	Synchronization to MPI • Type • Interval	 None/as master/as slave 1 s/10 s/1 min/10 min/1 h/12 h/24 h
	Correction factor	−10000 to +10000
Retentivity	Number of memory bytes starting with MB 0	0 to 255
	Number of S7 timers starting with T 0	0 to 255
	Number of S7 counters starting with C 0	0 to 255
Time-of-day interrupts	OB 10 activation	Yes/no
	OB 10 execution	• None • Once • Every minute • Hourly • Daily • Weekly • Monthly • Last day of the month • Annually
	Start date for the OB 10	Year-month-day

Table 7-16 Parameter blocks, settable parameters and their ranges for the BM 147 CPU

Parameter blocks	Settable parameters	Range
	Start time for the OB 10	Hours:minutes
Cyclic interrupts	Periodicity of the OB 35 (ms)	1 to 60000
Cycle/clock memory	Scan cycle monitoring time (ms)	1 to 6000
	Cycle load from communication (%)	10 to 50
	OB85 call at I/O access error	• For each access • For incoming and outgoing errors • No call
	Clock memory	Yes/no
	Memory byte	0 to 255
Protection	Level of protection	• 1: Key switch • 2: Write protection • 3: Write/readprotection
	Mode	• Process mode: permissible cycle increase (ms) from 3 to 65535 • Test mode
Communication	PD communication	1 to 11
	OP communication	1 to 11
	S7 basic communication	0 to 10

When does the CPU ”accept” the parameters?

The CPU accepts the parameters (configuration data) you have set:

- After POWER ON or a memory reset of the inserted memory module
- After the configuration data has been transferred without errors to the CPU online in STOP mode

Cycle and Response Times

8

Introduction

In this chapter you will learn what the cycle time and response time of the ET 200X with the BM 147 CPU consist of.

You can use the PD to read out the cycle time of your user program (see the *STEP 7 user manual*).

The response time is more important for the process. In this chapter we will show you in detail how to calculate the response time.

Chapter overview

Execution times

- For the *STEP 7* instructions that can be processed by the CPUs can be found in the *Instruction list*.
- For the SFCs/SFBs integrated in the CPUs can be found in the *Instruction list*.

8.1 Cycle time

Cycle time – a definition

The cycle time is the time that the operating system requires to process a program cycle – i.e. an OB 1 cycle – as well as all the program sections and system activities interrupting this cycle.

This time is monitored.

Components of the cycle time

Factors	Remarks
Operating system execution time	See Table 8-1
Process image transfer time (PII and PIQ)	See Table 8-2
User program execution time	Is calculated from the execution times of the individual instructions and a CPU-specific factor (for BM 147 CPU: 1.1).
Loading through interrupts	See Table 8-3

The following figure shows the components that make up the cycle time:

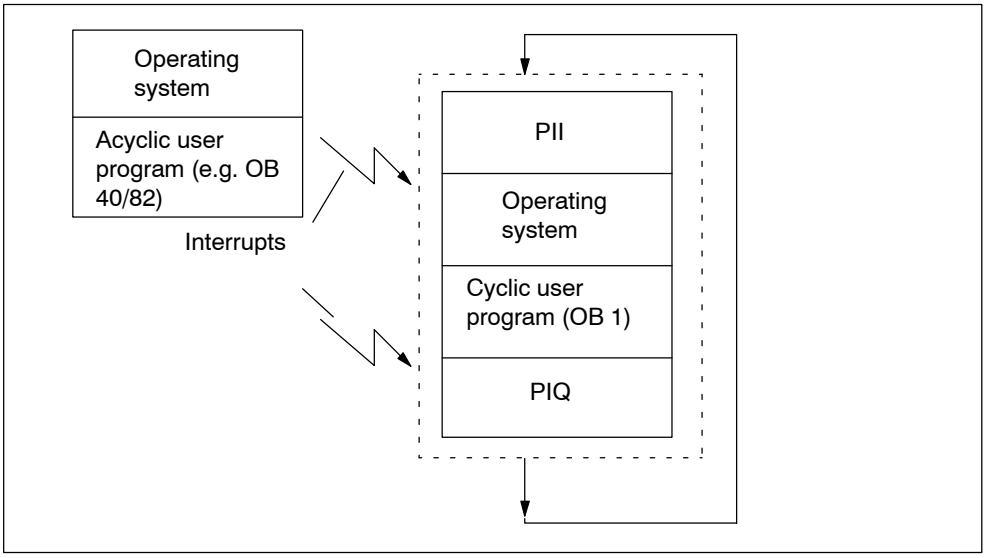


Figure 8-1 Component parts of the cycle time

Extending the cycle time

Note that the cycle time of a user program is extended by the following:

- Time-controlled interrupt handling
- Process interrupt handling (see also Section 8.3)
- Diagnostics and error handling (see also Section 8.3)

Operating system processing time

The operating system execution time for the BM 147 CPU is found in Table 8-1.

The specified time does not include the execution of:

- Testing and commissioning functions such as status/control of variables or block status
- Functions: Load block, delete block, compress block
- Communication
- Writing and reading the MMC with SFC 82 to 84

Table 8-1 Operating system processing time in the scan cycle checkpoint

Sequence	BM 147 CPU
Operating system processing time	500 µs

Process image transfer time

The table below contains the CPU times for process image updating (process image transfer time). The specified times can be longer as a result of interrupts that occur or by communication involving the CPU component of the BM 147 CPU.

(Process image = PI)

The CPU time for process image updating is calculated as follows:

K + A + D = Process image transfer time, in which K, A and D equal the following:

Table 8-2 Process image updating

	Designation	Times in BM 147 CPU
K	Base load	100 µs
Q	Bytes in the PI for the ET 200X I/O	35 µs per byte
D	Per word in the DP area	1 µs

Dependency of the user program scanning time

Simultaneously to actually executing the user program, the operating system of your CPU performs additional processes (e.g. timer management of core operating system). These processes prolong the execution time of the user program.

For the BM 147 CPU, multiply the execution time of your user program by a **factor of 1.1**.

Delay of the inputs and outputs

You have to take into account the following delay times, depending on the expansion module:

- For digital inputs: The input delay time
- For digital outputs: Negligible delay times
- For analog inputs: Cycle time of the analog input
- For analog outputs: Response time of the analog output

Extending the cycle by nesting interrupts

Table 8-3 shows typical extensions of the cycle time through nesting of an interrupt. The program runtime at the interrupt level must be added to these. If several interrupts are nested, the corresponding times need to be added.

Table 8-3 Extending the cycle by nesting interrupts

Interrupts	BM 147 CPU
Process interrupt	500 µs
Diagnostic interrupt	600 µs
Time-of-day interrupt	400 µs
Delay interrupt	300 µs
Watchdog interrupt	150 µs
Status interrupt/update interrupt/manufacturer-specific interrupt [1)]	600 µs
Programming/access error/runtime system error	400 µs

1) For BM 147-2 CPU only

8.2 Response time

Response time for ET 200X with BM 147 CPU

The response time is the time from the detection of an input signal at the ET 200X with the BM 147 CPU to the modification of an associated output signal via the inputs and outputs of the expansion modules.

Factors

The response time depends on the cycle time and the following factors:

Factors	Remarks
Delay of the inputs and outputs	You can find the delay times in the technical specifications of the expansion modules in the *ET 200X Distributed I/O Device* manual.

Range of fluctuation

The actual response time lies between a shortest and a longest response time. You must always reckon on the longest response time when configuring your system.

The shortest and longest response times are considered below to let you get an idea of the width of fluctuation of the response time.

Shortest response time

The following figure shows you the conditions under which the shortest response time is obtained.

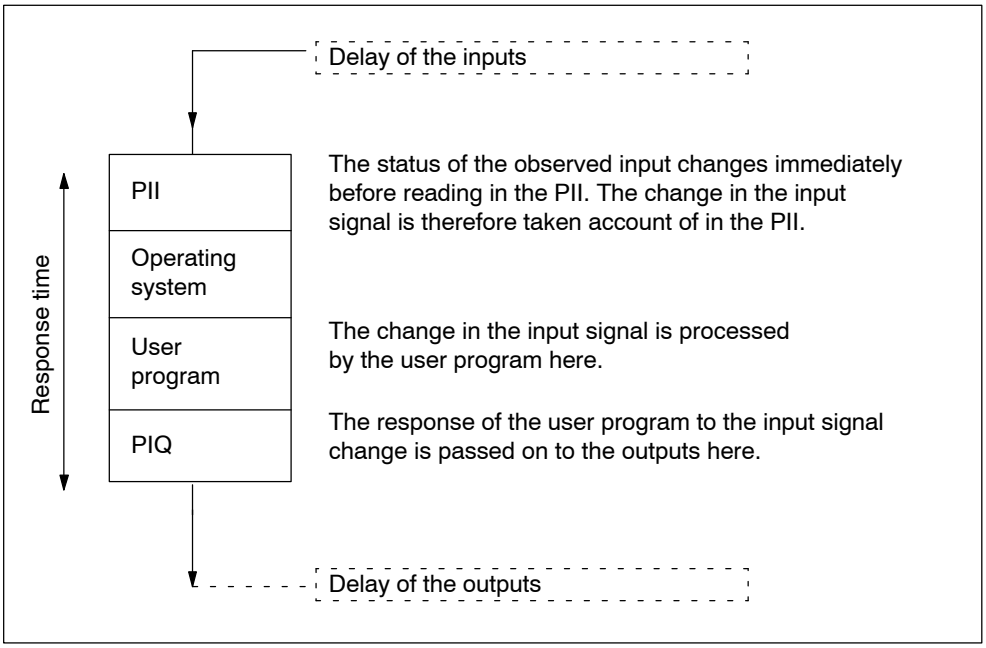


Figure 8-2 Shortest response time

Calculation

The (shortest) response time consists of the following:

- 1 × process image transfer time for the inputs +
- 1 × operating system processing time +
- 1 × program scanning time +
- 1 × process image transfer time for outputs +
- Delay of the inputs and outputs

This corresponds to the sum of the cycle time and the delay of the inputs and outputs.

Longest response time

The following figure shows what the longest response time consists of.

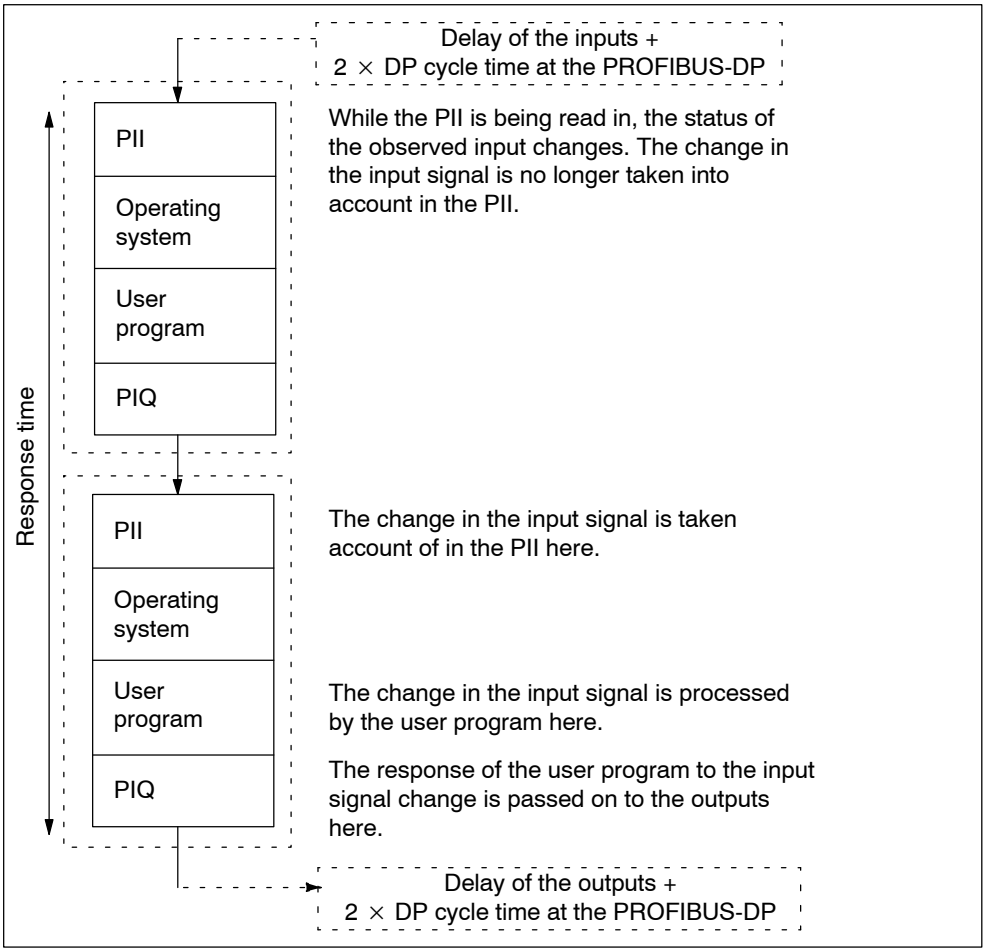


Figure 8-3 Longest response time

Calculation

The (longest) response time consists of the following:

- 2 × process image transfer time for the inputs +
- 2 × process image transfer time for the outputs +
- 2 × operating system processing time +
- 2 × program scanning time +
- 4 × run time of the DP slave frame (incl. processing in the DP master) +
- Delay of the inputs and outputs

This corresponds to the sum of 2x cycle time and delay of the inputs and outputs plus 4x DP cycle time.

8.3 Interrupt response time

Interrupt response time – a definition

The interrupt response time is the time from the first occurrence of an interrupt signal to the call of the first instruction in the interrupt OB of the BM 147 CPU.

The following generally applies: Interrupts of higher priority have precedence. This means that the program processing time of the higher-priority interrupt OB and of the not yet processed interrupt OBs of the same priority which occurred previously (queue) is added to the interrupt response time.

Interrupt response times

Table 8-4 Interrupt response times of the BM 147 CPU (without communication)

Interrupt response times (without communication) for...	Duration	
	min.	max.
Process interrupt	0.4 ms	0.7 ms
Diagnostics interrupt	0.4 ms	1.0 ms

Process interrupt handling

Process interrupt handling begins when the process interrupt OB 40 is called. Higher-priority interrupts cause the process interrupt handling routine to be interrupted. Direct accesses to the I/Os are made at the execution time of the instruction. After process interrupt handling has been completed, either cyclic program scanning is continued or additional interrupt OBs of the same priority or a lower priority are called and processed.

8.4 Calculation examples

8.4.1 Calculation examples for the cycle time and response time

Sample configuration

You have configured an ET 200X with the following modules:

- 1 BM 147 CPU basic module
- 2 EM 141 DI 8 × DC 24 V expansion modules (4 bytes each in the PI)
- 2 EM 142 DO 4 × DC 24 V/0.5A expansion modules (4 bytes each in the PI)

The user program has a runtime of 1.5 ms. Communication takes place only to the DP master.

Component parts of the cycle time

As a reminder: The cycle time consists of the following

- Operating system processing time +
- Process image transfer time +
- User program processing time +
- Loading through interrupts

Calculation

In this example, the cycle time is obtained from the following times:

- Operating system processing time in the scan cycle checkpoint:

  Approx. **0.5 ms**
- Process image transfer time

  Process image of the inputs: 100 µs + 8 bytes × 35 µs = approx. **0.38 ms**

  Process image of the outputs: 100 µs + 8 bytes × 35 µs = approx. **0.38 ms**
- User program processing time:

  Approx. 1.5 ms × factor specific to basic module 1.1 = approx. **1.65 ms**

Cycle time = 0.5 ms + 0.38 ms + 0.38 ms + 1.65 ms = **approx. 2.9 ms**.

Components of the response time

As a reminder: The longest response time is the sum of

- 2 × process image transfer time for the inputs +
- 2 × process image transfer time for the outputs +
- 2 × operating system processing time +
- 2 × program scanning time +
- Delay times of inputs and outputs

Calculation

Tip: Simple calculation: calculated cycle time × 2 + delay times of inputs and outputs.

The following therefore applies to the sample configuration (where the delay time of the outputs can be disregarded):

Response time = 2.9 ms × 2 + 8 × 4.8 ms = **approx. 44.2 ms**

8.4.2 Calculation example for the interrupt response time

Sample configuration

You have configured an ET 200X with the following modules:

- 1 BM 147 CPU basic module
- An EM 141 DI 8×DC 24 V expansion module

When you set the parameters for the BM 147 CPU, you only released the process interrupt. You decided not to use diagnostics or error handling. The expansion module has an input delay of 4.8 ms. No action is necessary at the cycle checkpoint. No communication takes place.

Calculation

The process interrupt response time in this example is obtained from the following times:

- Process interrupt response time of the BM 147 CPU: approx. 0.7 ms
- Internal interrupt preparation time: 0.25 ms
- Input delay: 4.8 ms

The process interrupt response time is calculated from the sum of times:

Process interrupt response time = 0.7 ms + 0.25 ms + 4.8 ms = **approx. 5.75 ms**.

This process interrupt response time elapses from the time a signal is applied to the digital input until the first instruction in OB 40.

Technical Specifications

9

In this chapter

In this chapter you will find:

- The technical data of basic module BM 147 CPU

9.1 Technical specifications of the BM 147 CPU

Order numbers

BM 147-1 CPU basic module:	6ES7 147-1AA10-0XB0
BM 147-2 CPU basic module:	6ES7 147-2AA00-0XB0
SIMATIC micro memory card (MMC): (see Section 7.3)	6ES7 953-8Lxx0-0AA0

Features

Basic module BM 147 CPU has the following features:

- Intelligent slave with RS 485 interface to the PROFIBUS-DP
- Stand-alone operation (MPI) possible
- 48 kByte working memory, non-expandable, retentive with inserted MMC
- Plug-in load memory on the MMC, up to 8 MBytes
- Powerfail-proof storage of the user program and configuration via MMC
- Programmable with *STEP 7*, V5.2 or higher + Service Pack 1
- Service-free
- No integrated I/O devices
- Maximum configuration of the local I/Os:
  7 expansion modules of the ET 200X spectrum

In addition to the features listed above, basic module BM 147-2 CPU also offers DP master functionality. Up to 32 DP slaves can be connected to the DP master interface.

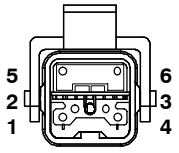
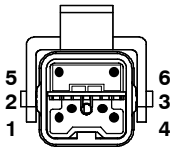
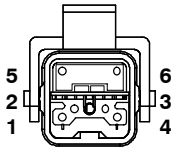
General technical specifications

The BM 147 CPU meets the general technical specifications of the ET 200X distributed I/O device. You will find these standards and test specifications in the chapter entitled ”General Technical Specifications” in the *ET 200X Distributed I/O Device* manual.

Use in direct sunlight is not permissible (due to excessive heating of the device).

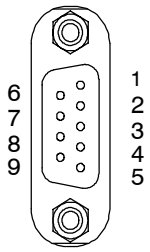
Pin assignment for BM 147 CPU

Table 9-1 Pin assignment of basic module BM 147 CPU

DP-M (X04) – for BM 147-2 CPU only –	**DP-IN** (X01)	**DP-OUT** (X02)
DP master interface (Output)	DP slave (Feed)	DP slave (Loop through)
		
View of the ECOFAST connections of basic module BM 147 CPU		

1	1L+ (NS)	Non-switched supply voltage for electronics/sensors (1L+)
2	1M (NS)	Ground to non-switched supply voltage for electronics/sensors (1L+)
3	2M (S)	Ground to switched load voltage (2L+)
4	2L+ (S)	Switched load voltage (2L+)
5	Signal A	PROFIBUS-DP
6	Signal B	PROFIBUS-DP

PD interface
(X03; MPI)



RS 485 interface

Pin	Signal	Description
1	–	–
2	–	–
3	RxD/TxD-P	Data line B
4	RTS	Request To Send
5	M	Galvanically isolated 5 V ground for PD interface
6	5 V	Galvanically isolated 5 V supply for PD interface
7	–	–
8	RxD/TxD-N	Data line A
9	–	–

Basic circuit diagram for the BM 147 CPU

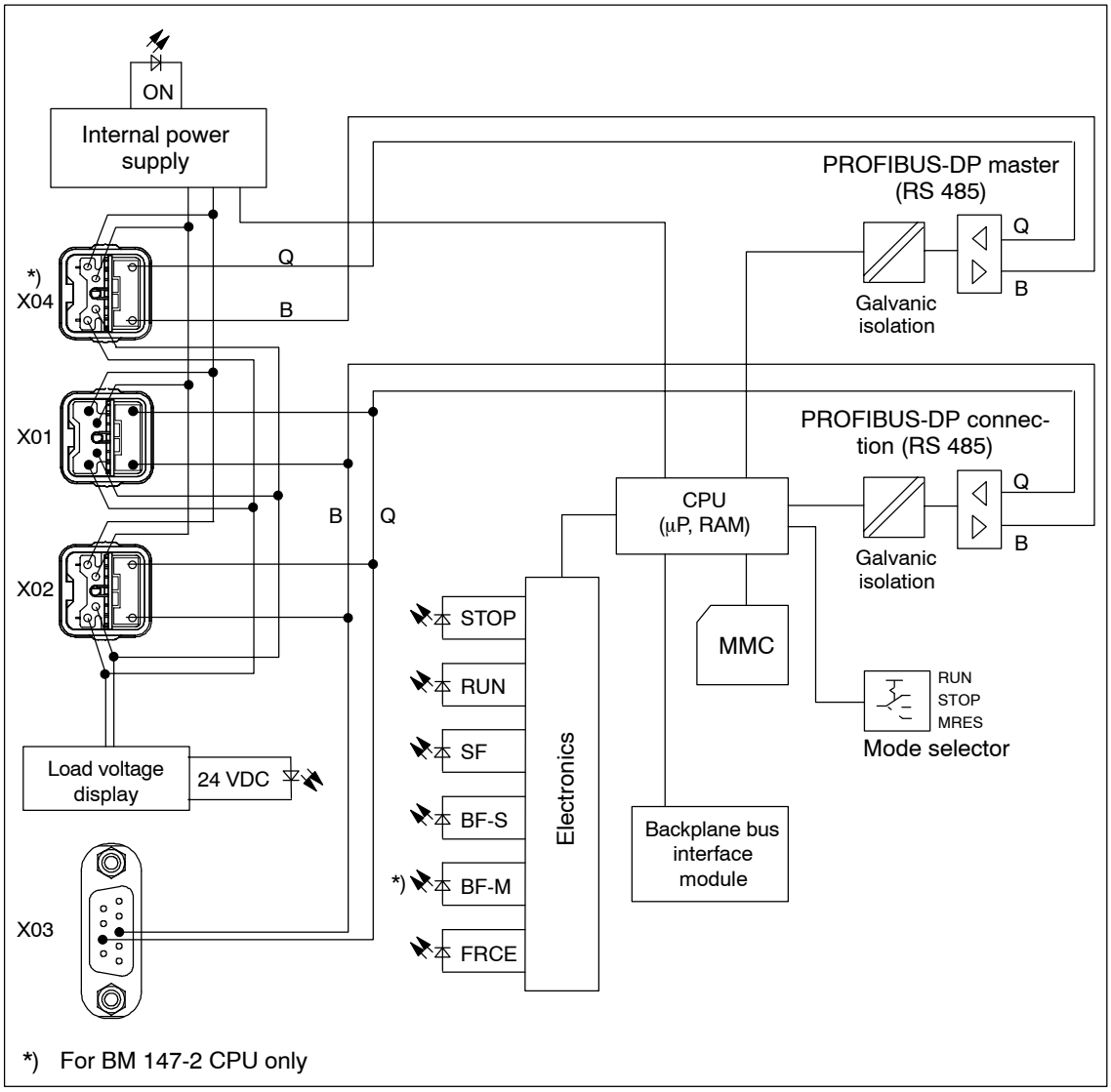


Figure 9-1 Block diagram BM 147 CPU

BM 147 CPU dimensioned drawing

The following figure shows the dimensioned drawing of basic modules BM 147-1 CPU and BM 147-2 CPU with ECOFAST connectors.

The bending radius of the ECOFAST hybrid cable at the specified height must be added.

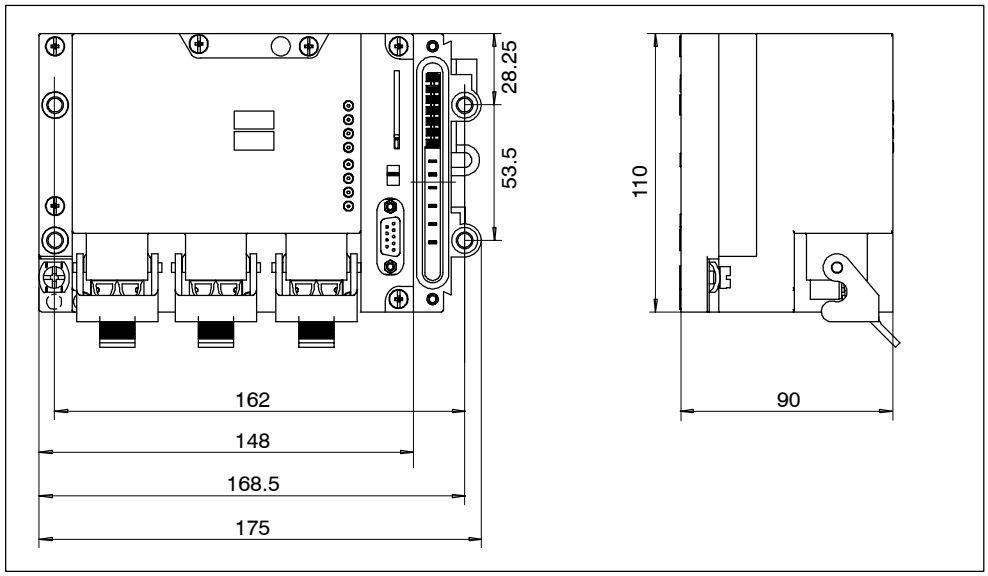


Figure 9-2 Dimensioned drawing of basic module BM 147 CPU (BM 147-2 CPU is shown)

Technical specifications

CPU and product version	
MLFB	BM 147-1 CPU: 6ES7 147-1AA10-0XB0 BM 147-2 CPU: 6ES7 147-2AA00-0XB0
• Hardware version	01
• Firmware version	V2.1.0
• Matching programming package	STEP 7 as of V5.2 + SP1
Memory	
Working memory	
• Integral	48 kBytes
• Expandable	No
Load memory	Plug-in (MMC up to 8 MB)
• Data storage on the MMC (after the last programming)	At least 10 years
Backup	Guaranteed by MMC (maintenance-free)
Processing times	
Processing times for	
• Bit instructions	Min. 0.1 µs
• Word instructions	Min. 0.2 µs
• Fixed-point math instructions	Min. 2 µs
• Floating-point math instructions	Min. 6 µs
Timers, counters and their retentive features	
S7 counters	256
• Retentivity	Adjustable
• Preset	From C 0 to C 7
• Counting range	0 to 999
IEC counters	Yes
• Number	Unlimited (limited only by the working memory)
• Type	SFB
S7 timers	256
• Retentivity	Adjustable
• Preset	No retentive timers
• Timing range	10 ms to 9990 s
IEC timers	Yes
• Number	Unlimited (limited only by the working memory)
• Type	SFB
Data areas and their retentive features	
Total retentive data area (incl. memory markers, timers, counters)	All
Memory markers	256 bytes
• Retentivity	Adjustable
• Preset	MB 0 to MB 15
Clock memory	8 (1 memory byte)
Data blocks	Max. 511 (DB 0 reserved)
• Size	Max. 16 kByte
Local data per priority class	Max. 510 bytes
Blocks	
Total	1024 (FBs + FCs + DBs)
FBs	Max. 512
• Size	Max. 16 kBytes
FCs	Max. 512
• Size	Max. 16 kBytes
DBs	Max. 511
• Size	Max. 16 kBytes
OBs	See *Instruction list*
• Size	Max. 16 kByte
Nesting depth:	
• Per priority class	8
• Additional levels within an error OB	4
Address areas (inputs/outputs)	
Total I/O address area	Max. 1024 bytes/1024 bytes
Process image	128 bytes/128 bytes (not adjustable)
Digital channels	Max. 8192
• Central	56/56
Analog channels	Max. 512
• Central	14/14

Time	
Clock	Hardware clock
• Buffered	Yes
• Backup time	Typ. 6 weeks (at ambient temperature of 40 °C)
• Accuracy	Deviation per day < 10 s
Run-time meter	1
• Number	0
• Range	0 to 2^{31} hours (when using the SFC 101)
• Selectivity	1 hour
• Retentive	Yes; must be restarted with every restart
Time synchronization	Yes
• In the PLC	Master
• On the MPI	Master/slave
S7 message functions	
Number of logon-able stations for signaling functions (e.g. OS)	Max. 12
Process diagnostic messages	ALARM_S, ALARM_SC, ALARM_SQ
• Simultaneously active Alarm_S blocks	Max. 40
Testing and commissioning functions	
Status/modify variables	Yes
• Variable	Inputs, outputs, memory markers, DBs, timers, counters
• Number of variables	Max. 30
– Of which status variables	Max. 30
– Of which modify variables	Max. 14
Force	Yes
• Variable	Inputs, outputs
• Number	Max. 10
Monitor block	Yes
Single sequence	Yes
Breakpoint	2
Diagnostic buffer	Yes
• Number of inputs	Max. 100 (not adjustable)

Communication functions	
PD/OP communication	Yes
Global data communication	Yes
• Number of GD packets	Max. 4
– Sender	Max. 4
– Receiver	Max. 4
• Size of GD packets	Max. 22 bytes
– Number of which consistent	22 bytes
S7 basic communication	Yes
• User data per job	Max. 76 bytes
– Number of which consistent	76 bytes (XSEND/XRCV) 64 bytes (XPUT/XGET) as server
S7 communication	Yes (server)
• User data per job	Max. 180 bytes
– Number of which consistent	64 bytes
S5-compatible communication	No
Standard communication	No
Number of connections	Max. 12
Used for	
• PD communication	Max. 11
– Reserved (default)	1
• OP communication	Max. 11
– Reserved (default)	1
• S7 basic communication	Max. 10
– Reserved (default)	0
Routing	Max. 4 (for BM 147-2 CPU only; the slave interface must be active)

Interface	
Slave interface	
Type of interface	Coexistent, integrated RS 485 interface
Physical system	RS 485
Galvanically isolated	Yes
Functionality	
• MPI	Yes
• PROFIBUS-DP	DP slave (active/passive)
• Point-to-point connection	No
MPI	
• Number of connections	12
• Utilities:	
– PD/OP communication	Yes
– Routing (BM 147-2 CPU only)	Yes
– Global data communication	Yes
– S7 basic communication	Yes
– S7 communication	Yes (only server)
• Transmission rates	Max. 12 Mbaud
DP slave	
• Number of connections	12 (each BM 147 CPU)
• Utilities:	
– PD/OP communication	Yes
– Routing (BM 147-2 CPU only)	Yes (only with active interface)
– Direct communication	Yes
• Transmission rates	Up to 12 Mbaud
• Automatic transmission rate search	Yes (only with passive interface)
• Intermediate memory	244 I bytes/244 O bytes
– Address areas	32 with a maximum of 32 bytes each *
• DPV1	No
• DDB (Device Database) file	You can find the current device master file at `http://www.ad.siemens.de/csi_e/gsd.`
Master interface (BM 147-2 CPU only)	
Type of interface	Integrated RS 485 interface
Physical system	RS 485
Galvanically isolated	Yes
Functionality	
• MPI	No
• PROFIBUS-DP	DP master
• Point-to-point connection	No
DP master	
• Number of connections	12 (each BM 147 CPU)
• Utilities:	
– PD/OP communication	Yes
– Routing	Yes
– Global data communication	No
– S7 basic communication	No
– S7 communication	Yes (only server)
– Direct communication	Yes
– Clock synchronism	Yes
– SYNC/FREEZE	Yes
– Activate/deactivate DP slaves	Yes
– DPV1	Yes
• Transmission rates	Up to 12 Mbaud
• Number of DP slaves per station	32
• Address area	Max. 1 kByte I/ 1 kByte O
• User data per DP slave	Max. 244 I bytes/ 244 O bytes

Programming	
Programming language	STEP 7 (LAD, FBD, STL)
Stored instructions	See *Instruction list*
Nesting levels	8
System functions (SFCs)	See *Instruction list*
System function blocks (SFBs)	See *Instruction list*
User program security	Yes
Dimensions and weight	
Installation dimensions W × H × D (mm)	175 x 110 x 90
Weight	Approx. 700 g
Voltages, currents, potentials	
Non-switched supply voltage for electronics/sensors (1L+)	24 VDC
• Permissible range	20.4 to 28.8 V
• Max. permissible feed current for supply voltage (1L+)	Up to 40 °C 10 A to 55 °C 8 A
• Polarity reversal protection	No
• Short-circuit protection	Yes, internal (thermally reversible) No, for looping through
• Voltage failure buffering	No
Switched load voltage (2L+)	24 VDC
• Permissible range	20.4 to 28.8 V
• Max. permissible feed current for load voltage (2L+)	Up to 40 °C 10 A to 55 °C 8 A
• Polarity reversal protection	No
• Short-circuit protection	No

Galvanic isolation	
• Between the supply voltage (1L+) and the load voltage (2L+)	Yes
• Between the load voltage (2L+) and all other circuit components	Yes
• Between PROFIBUS-DP and all other circuit components	Yes
• Between the non-switched supply voltage (1L+) and PROFIBUS-DP	Yes
• Between the PROFIBUS-DP slave and PROFIBUS-DP master	Yes
Permitted potential difference	
• Between different circuits	75 VDC, 60 VAC
Insulation tested at	500 VDC
Current consumption from the non-switched supply voltage (1L+)	• Typ. 85 mA • Max. 160 mA
Power loss of module	Typ. 3 W

* Up to the maximum size of the intermediate memory

Changing from BM 147 CPU (6ES7 147-1AA01-0XB0) to BM 147-1 CPU or BM 147-2 CPU

10

If you download your existing user program for the BM 147 CPU (6ES7 147-1AA01-0XB0) to a BM 147-1 CPU or BM 147-2 CPU (6ES7 147-xAAx0-0XB0), you may encounter the following problems:

The SFC 56, SFC 57 and SFC 13 may work asynchronously

A number of asynchronous SFCs are always processed or, under certain conditions, already processed following the first call (”quasi-synchronous”) on the BM 147 CPU (6ES7 147-1AA01-0XB0)

These SFC run truly asynchronously on the BM 147-1 CPU or BM 147-2 CPU (6ES7 147-xAAx0-0XB0). The asynchronous processing may continue for several OB 1 cycles. As a result, a queue within an OB may become a continuous loop.

- SFC 56 ”WR_DPARM”; SFC 57 ”PARM_MOD”

  These SFC always run “quasi-synchronously” on a standalone BM 147 CPU (6ES7 147-1AA01-0XB0).
  They run asynchronously on standalone BM 147-1 CPU or BM 147-2 CPU (6ES7 147-xAAx0-0XB0) and on distributed BM 147-1 CPU or BM 147-2 CPU.

Note

If you use the SFC 56 ”WR_DPARM” or SFC 57 ”PARM_MOD”, you should always evaluate the BUSY bit of the SFCs.

- SFC 13 ”DPNRM_DG”

  This SFC always runs “quasi-synchronously” when called in OB 82.
  It generally runs asynchronously on BM 147-1 CPU or BM 147-2 CPU (6ES7 147-xAAx0-0XB0).

Note

In the user program, all that should take place is that the task should be called in the OB 82. The evaluation of the data, which should take into account the BUSY bits and the acknowledgement in the RET_VAL, should take place in the cyclic program.

Tip:
With BM 147-1 CPU or BM 147-2 CPU we recommend using the SFB 54 instead of the SFC 13.

SFC 20 ”BLKMOV”

Previously this SFC could also be used to copy data from a non-process-related DB.

The SFC 20 no longer has this functionality. The SFC 83 ”READ_DBL” must now be used for this purpose.

SFC 54 ”RD_DPARM”

This SFC is no longer available. The asynchronous SFC 102 ”RD_DPARA” must be used instead.

SFCs which may give different results

If you only use logical addressing in your user program, you can ignore the following points.

If you use address conversions in the user program (SFC 5 ”GADR_LGC”, SFC 49 ”LGC_GADR”), you must check the slot assignment and logical start address assignment for DP slaves.

- The diagnostic address of the DP slave is now always assigned to slot 0 (station proxy).
- The DP slave is integrated in *STEP 7*:

  The basic module (slot 2) may have its own address
  (e.g. BM 147-1 CPU or BM 147-2 CPU as Intelligent Slave).

Changed runtimes during program processing

If you have created a user program that is optimized for the execution of certain processing times, it is important to note the following when using the BM 147-1 CPU or BM 147-2 CPU:

- Program processing in BM 147-1 CPU or BM 147-2 CPU is significantly faster.
- Functions that require MMC access (e. g. system runup, program download in RUN, DP station recovery, etc.), may run slower on the BM 147-1 CPU and BM 147-2 CPU.

Changing the diagnostic addresses of DP slaves

It is important to note that the diagnostic addresses for the slaves may have to be reassigned in some cases since two diagnostic addresses per slave are sometimes required due to adaptation to the DPV1 standard.

- The virtual slot 0 has its own address (diagnostic address of the station proxy).

  The module state data for this slot (read out with SFC 51 ”RDSYSST”) contains the identifiers which affect the complete slave/station, e.g. the ”Station Faulty” identifier. The station failure and station recovery are also signaled in the OB 86 of the master via the diagnostic address of the virtual slot 0.
- Furthermore, slot 2 also has its own address in the case of modules integrated in *STEP 7* (e.g. BM 147-1 CPU or BM 147-2 CPU as I-slave). This address is used to signal the change in operating state in the diagnostic interrupt OB 82 of the master, e.g. with BM 147-1 CPU or BM 147-2 CPU as I-slave.

Note

Reading out the diagnosis with SFC 13 “DPNRM_DG”:

The diagnostic address originally assigned still functions. Internally, *STEP 7* assigns slot 0 to this address.

If you use the SFC 51 ”RDSYSST” to read out, for example, module state information or rack/station state information, you must also take the changed meaning of the slots and the additional slot 0 into consideration.

Using consistent data areas in the process image with DP slaves

Below is a list of the points to which you must pay attention with communication in a DP master system if you want to transfer I/O areas with the ”Total Length” consistency.

- If the address area of consistent data is in the process image, this area is updated automatically.
- You can also use the SFCs 14 and 15 to read and write consistent data.
- If the address area for consistent data is outside the process image, you must use the SFCs 14 and 15 to read and write consistent data.
- It is also possible to address the consistent areas directly (for example, L PIW or T PQW).

You can transfer a maximum of 32 bytes of consistent data.

PD/OP functions

In the BM 147 CPU (6ES7 147-1AA01-0XB0), PD/OP functions at the DP interface were only possible at an active interface.
In the BM 147-1 CPU and BM 147-2 CPU (6ES7 147-xAAx0-0XB0), these functions are possible at both passive and active interfaces. However, the performance at the passive interface is noticeably lower.

Routing in BM 147-2 CPU as intelligent slave

If you use the BM 147-2 CPU as an intelligent slave, the routing function can only be used when the slave interface is active and the DP master interface has been parameterized.
To do so, activate the Commissioning/Test Mode checkbox in the DP interface properties in *STEP 7*.

New functionalities of the BM 147-1 CPU and BM 147-2 CPU (6ES7 147-xAAx0-0XB0)

- The node address (PROFIBUS-DP and MPI) no longer has to be set.
- The PROFIBUS-DP connectors are designed in ECOFAST technology (see Chapter 5).
- Coexistent interface MPI/DP (active/passive) (see Chapter 7.5)
  A PD can be connected directly to the new MPI interface.
- Additional DP master interface for BM 147-2 CPU (see Chapter 7.5)
- New memory concept (see Section 7.4)
- Global data communication (see Section 7.8)

  This utility is used to enable the cyclic exchange of global data between SIMATIC S7-CPUs (and therefore also the BM 147-1 CPU and BM 147-2 CPU).
- S7 basic communication (see Section 7.8)

  This utility is used to enable data exchange between the BM 147-1 CPU or BM 147-2 CPU and communications-capable SIMATIC modules within an S7 station. The SFCs 65 to 74 are provided to support this.
- MMC up to 8 MBytes (see Section 7.3)
- Data storage (see Section 7.4.4)

  The data is stored on an MMC and then downloaded back to the CPU using the SFCs 82 to 84.
- Storage of the STEP 7 project on an MMC (see Section 7.4.5)
- New SFBs

  The SFBs 52 to 54 and SFB 75 to IEC 61784-1 are supported.
- 32-bit run-time meter

  The meter is operated using the SFC 101.
- Routing
- Non-retentive DBs (generated with SFC 82 or in *STEP 7*) (see Chap. 7.4.1)

Master functionality of the BM 147-2 CPU

Activation/deactivation of DP slaves via the SFC 12
Slaves that were deactivated via the SFC 12 are automatically activated in a restart for the BM 147-2 CPU (transition from STOP to RUN).

Interrupt events from the distributed I/O while the CPU is in STOP mode
Due to the new DPV1 functionalities (IEC 61784-1:2002 Ed1 CP 3/1), how incoming interrupt events from the distributed I/O while the CPU is in STOP mode are handled also changes.
In BM 147-2 CPU, an interrupt event (process, diagnostic interrupt, new DPV1 interrupt) from the distributed I/O while the CPU is in STOP mode is already acknowledged and, if applicable, entered in the diagnostic buffer (diagnostic interrupt only). In the subsequent change of the CPU into RUN mode, the interrupt is no longer processed via the corresponding OB. Possible faults in slaves can be read out via corresponding SZL information (e. g. SZL 0x692 read out via SFC 51).

Position of the BM 147 CPU in the CPU Range

11

In this chapter, you will find out the most important differences to two selected CPUs in the S7-300 SIMATIC family.

More information

You can find further information on how to create and structure programs in the *STEP 7* manuals and *online help*.

11.1 Differences to selected S7-300 CPUs

The following table lists the most important programming differences between two selected CPUs of the S7-300 SIMATIC family and the BM 147 CPU.

Table 11-1 Differences to selected S7-300 CPUs

Features	CPU 315-2 DP	CPU 315-2 DP (modular)	BM 147 CPU	
			(6ES7 147-1AA01-0XB0)	(6ES7 147-xAAx0-0XB0)
Real-time clock	Hardware	Hardware	Software	Hardware
Memory backup	Yes, with battery	Guaranteed by MMC (maintenance-free)	Not possible	Guaranteed by MMC (maintenance-free)
Memory card	Memory card	MMC	No	MMC
Number of connections to PD and OP	4 (as of 10/99: 12)	16	5	max. 12
Setting the PROFIBUS address	Hardware configuration	Hardware configuration	Hardware configuration must match address setter	Hardware configuration
Transmission rate to PD and OP	187.5 kbaud (MPI) 12 Mbaud (DP)	187.5 kbaud (MPI) 12 Mbaud (DP)	12 Mbaud (DP)	12 Mbaud (MPI/DP)
Communication:				
PD/OP	Yes	Yes	Yes	Yes
Global data comm.	Yes	Yes	No	Yes
S7 basic comm.	Yes	Yes	Yes (server)	Yes
S7 comm.	Yes (server)	Yes (server)	Yes (server)	Yes (server)
Direct communication	Yes	Yes	No	Yes
Range of uses with DP	As a DP master As a DP slave Stand-alone	As a DP master As a DP slave Stand-alone	As a DP slave Stand-alone	As a DP slave As a DP master Stand-alone
Addressing	Free	Free	Slot-oriented	Free
Interrupt response time	0.4-1.3 ms	0.3-1.2 ms	0.8-1.8 ms	0.4-1.0 ms
Removal/insertion of modules during operation	No	No	No	No
Voltage failure bridging (5 ms)	Yes	Yes	Not available for reasons inherent to the system	

Order Numbers

A

Introduction

Below you will find the order numbers of the BM 147 CPU, of the Micro Memory Cards (MMC) and of accessories that you may require when using the ET 200X.

Basic modules

Table A-1 BM 147 CPU basic modules – order numbers

Description	Order number
BM 147-1 CPU basic module	6ES7 147-1AA10-0XB0
BM 141-2 CPU basic module	6ES7 147-2AA00-0XB0

SIMATIC Micro Memory Card (MMC)

Table A-2 Micro Memory Cards – order numbers

Description	Order number
MMC 64k	6ES7 953-8LF00-0AA0
MMC 128k	6ES7 953-8LG00-0AA0
MMC 512k	6ES7 953-8LJ00-0AA0
MMC 2M	6ES7 953-8LL00-0AA0
MMC 4M	6ES7 953-8LM00-0AA0
MMC 8M	6ES7 953-8LP10-0AA0

Accessories

Table A-3 Accessories – order numbers

Description	Order number
Cap (for covering unused ECOFAST sockets; 10 pieces)	6ES7 194-1JB10-0XA0
ECOFAST terminating resistor for PROFIBUS-DP	
1 piece	6GK1 905-0DA10
5 pieces	6GK1 905-0DA00
ECOFAST hybrid cable (2 copper conductors and 2 x 2 copper cables,∅ 1.5 mm^2) prefabricated with ECOFAST connector in various lengths:	
1.5 m	6XV1 830-7BH15
3.0 m	6XV1 830-7BH30
5.0 m	6XV1 830-7BH50
10.0 m	6XV1 830-7BN10
15.0 m	6XV1 830-7BN15
20.0 m	6XV1 830-7BN20
25.0 m	6XV1 830-7BN25
30.0 m	6XV1 830-7BN30
35.0 m	6XV1 830-7BN35
40.0 m	6XV1 830-7BN40
45.0 m	6XV1 830-7BN45
50.0 m	6XV1 830-7BN50
If you wish to assemble the hybrid cable yourself:	
• PROFIBUS ECOFAST Hybrid Plug 180 (ECOFAST Cu, quantity 5 pieces)	
Pin insert (for looping through)	6GK1 905-0CA00
Socket insert (for feed)	6GK1 905-0CB00
• ECOFAST hybrid cable, not prefabricated (2 copper conductors and 2 x 2 copper cables) in various lengths:	
20 m	6XV1 830-7AN20
50 m	6XV1 830-7AN50
100 m	6XV1 830-7AT10
• ECOFAST hybrid cable by the meter (2 copper conductors and 2 x 2 copper cables)	6XV1 830-7AH10
Plug-in cable for PROFIBUS (active PD plug-in cable) 12 MBaud for PD connection	6ES7 901-4BD00-0XA0

Glossary

1L+

Non-switched supply voltage for electronics/sensor
This voltage supplies the electronics and the sensors connected to the expansion modules.

2L+

Switched load supply voltage
This voltage supplies the actuators connected to the expansion modules.

Adress

An address is the designation for a certain address ID or address area (e.g. input I 12.1; memory word MW 25; data block DB 3).

AKKU

The accumulators are registers in the → CPU that act as an intermediate memory for loading and transfer operations as well as comparison, calculation and conversion operations.

Automation system

An automation system is a programmable logic controller that consists of at least one CPU, various input and output modules and human-machine interfaces.

Backup memory

The backup memory ensures that the memory areas of the → CPU that do not have a buffer battery are buffered. A parameterizable number of times, counters, markers and data bytes is buffered.

Bus

A bus is the common transmission route to which all nodes are connected; has two defined ends

For the ET 200, the bus is either a two-wire cable or a fiber optic cable.

Coexistent MPI/DP interface

The coexistent MPI/DP interface is **a single** logical interface that is physically available at one or several connectors. For basic module BM 147 CPU, the coexistent MPI/DP interface is available at 3 physical connectors (X01 to X03).

The ET 200X is integrated as a slave in an MPI or PROFIBUS-DP network via the coexistent MPI/DP interface of the BM 147 CPU.

Compression

Using the PD online function, ”Compression”, all valid blocks in the RAM of the CPU are pushed to the very beginning of the user memory without leaving gaps. This eliminates gaps that occur when blocks are deleted or corrected.

Consistent data

Data that belongs together with respect to its content and that must not be separated is referred to as consistent data.

For example, the values from analog modules must always be handled consistently, i.e. the value of an analog module must not be corrupted by reading it out at two different points in time.

Counter

Counters are components of the → system memory of the CPU. The content of the ”counter cells” can be modified by *STEP 7* instructions (e.g. count up/down).

CPU

Central Processing Unit = central module of the S7 automation system with a control and arithmetic logic unit, memory, operating system and interface for the programming device.

Cross communication

See Direct communication

Cycle time

The cycle time is the time taken by the → CPU to scan the → user program once.

Data block

Data blocks (DB) are data areas in the user program that contain user data. There are global data blocks that can be accessed from all code blocks and there are instance data blocks that are assigned to a specific FB call.

Device master file

A device master file contains all the DP slave-specific properties. The structure of the device master file (DDB) is defined in IEC 61784-1:2002 Ed1 CP 3/1.

Diagnosis

Diagnosis is the detection, localization, classification, display and further evaluation of errors, faults and messages.

Diagnosis offers monitoring functions that are executed automatically while the system is running. This increases the availability of the systems by reducing maintenance and standstill periods.

Diagnostic buffer

The diagnostic buffer is a buffered memory area in the CPU which stores the diagnostics events in the order in which they occurred.

Diagnostics interrupt

Diagnostics-capable modules use diagnostic interrupts to report system errors which they have detected to the central CPU.

In SIMATIC S7/M7: When an error is detected or disappears (e.g. wire break), the ET 200X triggers a diagnostic interrupt, provided the interrupt is enabled. The CPU of the DP master interrupts the execution of the user program or lower-priority priority classes and processes the diagnostic interrupt block (OB 82).

In SIMATIC S5: The diagnostic interrupt appears in the station diagnosis. Faults such as conductor breakage can be detected by means of a cyclic querying of the diagnostic bits in the station diagnosis.

Direct communication

Direct communication is a special communication relationship between PROFIBUS-DP nodes. Direct communication is characterized by the fact that the PROFIBUS-DP nodes ”listen in” to find out which data a DP slave is sending back to its DP master.

Distributed I/O devices

Distributed I/O devices are input/output devices that are not used in the central unit but set up at distributed locations at large distances from the CPU, e.g.:

- ET 200S, ET 200M, ET 200B, ET 200C, ET 200U, ET 200X, ET 200L
- DP/AS-I Link
- S5-95U with a PROFIBUS-DP slave interface
- Other DP slaves from Siemens or other manufacturers

The distributed I/O devices are connected with the DP master via the PROFIBUS-DP.

DP master

A → master that complies with IEC 61784-1:2002 Ed1 CP 3/1 is designated as a DP master.

DP slave

A → slave on the PROFIBUS bus system with the PROFIBUS-DP protocol that complies with IEC 61784-1:2002 Ed1 CP 3/1 is referred to as a DP slave.

DP standard

The DP standard is the bus protocol of the ET 200 distributed I/O system based on IEC 61784-1:2002 Ed1 CP 3/1.

DPV0

Cyclic data exchange between the DP master and the DP slaves.

DPV1

Expansion of the DPV0 to include acyclic data exchange between the DP master and the DP slaves.

Error handling via OB

If the operating system detects a specific error (e.g. an access error in the case of *STEP 7*), it calls the organization block (error OB) provided for this event that specifies the subsequent behavior of the CPU.

Error message

An error message is one of the possible responses of the operating system to a runtime error. The other possible responses are: → error response in the user program, STOP mode of the CPU.

Error response

Response to a → Runtime error. The operating system can respond in the following ways: conversion of the programmable controller to STOP mode, call of an organization block in which the user can program a response, or display of the error.

ET 200

The ET 200 distributed I/O system with the PROFIBUS-DP protocol is a bus for connecting distributed I/O devices to a CPU or an appropriate DP master.
ET 200 is characterized by a rapid response time, since only a small amount of data (bytes) is transmitted.

ET 200 is based on IEC 61784-1:2002 Ed1 CP 3/1.

ET 200 works according to the master-slave principle. Examples of DP masters are the IM 308-C master connection or the CPU 315-2 DP.

DP slaves can be the distributed I/O devices ET 200S, ET 200B, ET 200C, ET 200M, ET 200X, ET 200U, ET 200L or DP slaves from Siemens or other vendors.

FC → Function

FORCE

During commissioning, for example, the ”Force” function allows certain outputs to be set to ”ON” for any length of time, even if the logic operations of the user program are not fulfilled (e.g. because inputs are not wired).

FREEZE

FREEZE is a control command of the DP master to a group of DP slaves.

After the FREEZE control command is received, the DP slave freezes the current state of the **inputs** and transmits it cyclically to the DP master.

After each new FREEZE control command, the DP slave once again freezes the state of the **inputs**.

The input data is transmitted cyclically again from the DP slave to the DP master only after the DP master has sent the UNFREEZE control command.

Function

A function (FC) is, according to IEC 61131-3, a code block without statistical data. A function allows the transmission of parameters in the user program. Thus, functions are ideal for programming frequently recurring complex functions, such as calculations.

Intelligent DP slave

The defining feature of an intelligent DP slave is that input/output data is not made available to the DP master by a real input/output of the DP slave directly, but by a preprocessing CPU (in this case basic module BM 147 CPU).

Interrupt

The operating system of the CPU recognizes 10 different priority classes that control the processing of the user program. These include, among others, interrupts such as the diagnostics interrupt. When an interrupt occurs, the operating system automatically calls an associated organization block in which the user can program the required response (e. g. in an FB).

Interrupt, diagnosis → Diagnostics interrupt

Interrupt, process → Process interrupt

Load memory

The load memory is a component of the CPU. It contains objects generated by the programming device. It is implemented either as a plug-in memory card/micro memory card or a permanently integrated memory.

Marker

Markers are components of the → system memory of the CPU for storing intermediate results. They can be access on the basis of bits, bytes, words or double words.

Masse

Ground is the total of all interconnected inactive components of a device that are not able to carry a dangerous contact voltage even in the even of a malfunction.

Master

Masters may, when they are in possession of a token, send data to other nodes and request data from other nodes (= active nodes). DP masters are, for example, the CPU 315-2 DP or the IM 308-C.

Master system

All DP slaves that are assigned to a DP master for either reading or writing plus the DP master itself make up the master system.

MMC

Micro Memory Card. Memory module for SIMATIC systems. Can be used as a load memory and portable data carrier.

MPI

The multipoint interface (MPI) is the programming device interface of the SIMATIC S7.

Nesting depth

One block can be called from within another using block calls. The nesting depth is the number of code blocks that are called up simultaneously.

Node

Devices that send, receive or amplify data via the bus, e.g. DP master, DP slave, RS 485 repeater, active star coupler.

OB → Organization block

OB priority

The operating system of the CPU distinguishes between various priority classes, such as cyclic program scanning and process interrupt-driven program scanning. Each priority class → is assigned organization blocks (OB) in which the S7 user can program a response. The OBs have, by default, differing priorities that determine the order in which they are processed if they occur simultaneously or if they interrupt one another.

Operating mode

The SIMATIC S7 programmable controllers can detect the following operating modes: STOP, → START UP, RUN.

Operating system of the CPU

The operating system of the CPU organizes all functions and procedures of the CPU that are not linked to a specific control task.

Organization block

Organization blocks (OBs) form the interface between the operating system of the CPU and the user program. The sequence in which the user program is processed is defined in the organization blocks.

Parameters

1st variable of a *STEP 7* code block

2nd variable to set the behavior of a module (one or more per module). Each module possesses a useful basic setting upon delivery that can be modified by configuring it in *STEP 7*.

PD → Programming device

PLC → Programmable logic controller

Priority class

The operating system of an S7-CPU offers a maximum of 26 priority classes (or ”program processing levels”) to which different organization blocks are assigned. The priority classes determine which OBs will interrupt other OBs. If one priority class holds several OBs, the OBs do not interrupt each other but are processed sequentially.

Process image

The process image is part of the → system memory of the CPU. The signal states of the inputs are written into the process input image at the start of the cyclic program. At the end of the cyclic program, the signal states in the process output image are transferred to the outputs.

Process interrupt

A process interrupt is triggered by interrupt-triggering modules on the occurrence of a specific event in the process. The process interrupt is reported to the CPU. The associated →organization block is then processed in accordance with the priority of this alarm.

PROFIBUS

PROcess FIeld BUS, process and field bus standard that is defined in the IEC 61784-1:2002 Ed1 CP 3/1 standard. It specifies functional, electrical and mechanical characteristics of a bit serial field bus system.

PROFIBUS is available with the protocols DP (the German abbreviation for distributed I/O), FMS (= field bus message specification), PA (= process automation) or TF (= technology (process-related) functions).

PROFIBUS address

Each bus node must receive a PROFIBUS address to identify it uniquely on the PROFIBUS bus system.

The PC/PD has the PROFIBUS address ”0”.

The PROFIBUS addresses 1 to 125 are permissible for the ET 200X distributed I/O device.

Programmable logic controller

A programmable logic controller (PLC) is an electronic controller whose function is stored in the control unit as a program. The configuration and wiring of the device therefore is not determined by the function of the controller. The programmable logic controller is structured like a computer; it consists of a → CPU (central module) with a memory, input/output modules and an internal bus system. The I/O and the programming language are designed to meet the requirements of the control technology.

Programming device

Programming devices are basically personal computers that are suitable for the industrial environment, compact and transportable. They are characterized by a special hardware and software for SIMATIC programmable logic controllers.

Publisher

A sender in direct data communication. *See* Direct communication

Restart

When a CPU starts up (e. g. after the mode selector has been switched from STOP to RUN or in the case of a POWER ON), the organization block OB 100 (restart) is processed before cyclic program scanning (OB 1) takes place. In the event of a restart, the process image of the inputs is read in and the *STEP 7* user program is processed beginning with the first command in OB 1.

Runtime error

Error which occurs during processing of the user program on the programmable controller (i.e. not in the process).

Scan cycle checkpoint

The point during CPU program scanning at which the process image is updated, for example.

SFC → System function

Slave

A slave may only exchange data with a → master if prompted by the master to do so. Examples of slaves are all DP slaves such as ET 200S, ET 200B, ET 200X, ET 200M, etc.

Stand-alone operation

The device is operated on a stand-alone basis without data exchange to a superordinate master and without direct communication with other DP slaves. All the modules power up using default parameters and with the maximum configuration (8 slots, 64 bytes consistently).

Start event

Start events are defined events such as errors, times and interrupts. They cause the operating system to start an associated organization block (if programmed accordingly by the user). Start events are displayed in the header information of the associated OB. The user can respond to start events in the user program.

START

The STARTUP mode is run through when the system goes from the STOP mode to the RUN mode.

Can be triggered by the mode selector or after power on or an operator action on the programming device. In the case of the ET 200X a restart is carried out.

STEP 7

Programming language for developing user programs for SIMATIC S7 PLCs.

Subscriber

A recipient in direct communication. *See* Direct communication

SYNC

SYNC is a control command of the DP master to a group of DP slaves.

By means of the SYNC control command, the DP master causes the DP slave to freeze the current statuses of the **outputs**. For the following frames, the DP slave stores the output data but the states of the outputs remain unchanged.

After each new SYNC control command, the DP slave sets the outputs that it has stored as output data. The outputs are not updated cyclically again until after the DP master has sent the UNSYNC control command.

System diagnostics

System diagnostics is the detection, evaluation and notification of errors that occur within the automation system. Examples of such errors are program errors or module failures. System errors can be indicated by means of LED displays or in *STEP 7*.

System function

A system function (SFC) is a function integrated in the operating system of the CPU that can be called up in the *STEP 7* user program as required.

System memory

The system memory is integrated in the central module and designed as a RAM. The operand areas (e.g. times, counters, markers) and the data areas required internally by the operating system (e.g. buffer for communication) are stored in the system memory.

Timer → Times

Times

Times are components of the → system memory of the CPU. The contents of the ”timer cells” are updated automatically by the operating system asynchronously to the user program. With *STEP 7* instructions, the exact function of the time cell (e. g. switch-on delay) is defined and its processing (e. g. starting) is triggered.

Token

Access rights on bus

Total current

Sum of the currents of all output channels of a digital output module.

Transmission rate

The transmission rate is the data transmission speed and specifies the number of transmitted bits per second (transmission rate = bit rate).

In the case of the ET 200X, transmission rates of 9.6 kbaud to 12 Mbaud are possible.

User memory

The user memory contains code and data blocks of the user program. The user memory can be integrated in the CPU or can be provided on plug-in memory cards (BM 147 CPU) or memory modules. However, the user program is always processed from the → working memory of the CPU.

User program

SIMATIC differentiates between → the operating system of the CPU and user programs. The latter are created in the various programming languages (ladder diagram and instruction list) using the → *STEP 7* programming software and are stored in code blocks. Data is stored in data blocks.

Working memory

The working memory is a RAM in the → CPU on which the processor accesses the user program while the user program is being executed.

Index

D

E

F

G

H

I

L

M

N

O

P

R

S

T

U

W

SIEMENS

Product information for

11.2005

Manual Basic Module BM 147 CPU, Version 05/2003

Manual Interface Module IM 151-7 CPU, Version 11/2003

This product information contains important information about the documentation mentioned above. It is to be regarded as a separate component. Its specifications and information have a higher binding nature than those of other manuals and catalogs in case of discrepancies.

Larger working memory and extended number range for blocks

The working memory has been extended for the Basic Module BM 147 CPU and the Interface Module IM 151-7 CPU. The CPUs can now execute larger user programs.
You can now use the block numbers 0 to 2047 for FB and FC in the user programs.

The total amount of blocks (FBs + FCs + DBs) remain unchanged with max. 1024.

	BM 147-1 (6ES7 147-1AA11-0XB0)	**BM 147-2** (6ES7 147-2AA01-0XB0)	**BM 147-2** (6ES7 147-2AB01-0XB0)	**IM 151-7** (6ES7 151-7AA11-0AB0)
Working memory				
• Size • Expandable	64 KB No	64 KB No	128 KB No	64 KB No
Blocks (FB, FC)				
FB • Quantity • Number range	 Max. 512 FB 0 to FB 2047	 Max. 512 FB 0 to FB 2047	 Max. 512 FB 0 to FB 2047	 Max. 512 FB 0 to FB 2047
FC • Quantity • Number range	 Max. 512 FC 0 to FC 2047	 Max. 512 FC 0 to FC 2047	 Max. 512 FC 0 to FC 2047	 Max. 512 FC 0 to FC 2047

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Product information for
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