SIMATIC S5

Standard Function Counter for the IP 265

Manual

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Preface

Counting of high-speed processes is an essential task in automation. For this reason, SIEMENS offers a submodule with the standard function counter, MLFB 6ES5 840-4SH01.

The submodule with the standard function counter can be used together with an IP 265 in the S5-90U, S5-95U and S5-100U programmable controllers and additionally in the ET 200 system (from version Z02 of the IM 318-B).

The principle of operation of the IP 265 is determined by the use of the submodule with the standard function counter.

All interfaces to the standard function are the interfaces of the IP 265 to the SIMATIC environment or to the process I/O.

See the relevant section of your system manual for details of the construction of a system or the installation of the module.

Function overview of the standard function

Three different counter functions have been stored in the submodule. The functions can be divided into two areas:

- 2 counters with 16-bit data width These two counters can be used independently of one another as up counter (normal counter function) or as down counter (periodic counter function).
- 1 counter with 32-bit data width Both counters can be combined into one 32-bit wide counter (cascade function) for counter functions requiring a considerably larger data area. This counter operates as a down counter (like the periodic counter function).

From the STEP 5 program, you can set the relevant setpoints and control signals and read the relevant actual values and diagnostic signals over the I/O bus.

The following description refers exclusively to the principle of operation of the standard function counter in the IP 265.

Please see the descriptions in the IP 265 manual or in your system manual (S5-95U, S5-100U) for details of installation guidelines and connection methods.

Convention

Information of special importance is contained in framed boxes like the following:



See the Safety-Related Guidelines in your manual (IP 265) or your system manual (S5-95U) for the definition of the terms "Warning" and "Note".

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1 Construction of the IP 265 Module

1.1 Hardware design of the module

The standard function counter is carried by the IP 265, a single-width module of the S5-100 PLC. The IP 265 is equipped with several hardware interfaces for communication with the system environment.

Figure 1-1 shows the position of the interfaces and the operator controls on the frontplate of the module.



Figure 1-1. Overview of the Module

1.1.1 Terminal for Load Voltage

The load circuit of the plant controller is supplied with 24 V DC via the load voltage connector on the frontplate of the IP 265.

The 24 V supply allows connection of 24 V plant sensors and actuators to the digital inputs and outputs of the module (load current circuit).

Note

The IP 265 must receive the 24 V supply for operation.

1.1.2 Digital 24 V Inputs/Digital 24 V Outputs

Two 9-pin sub D interfaces are located on the frontplate of the IP 265

Connect the signal lines of the sensors to the 9-pin sub D connector marked "INPUT". You can connect up to 8 24 V digital inputs. The frequency of the input signals may be up to 10 kHz.

Connect the signal lines of the actuators to the 9-pin sub D socket marked "OUTPUT". The response time of the 24 V digital outputs depends on the resistive load of the output circuit and the type of output level changes (LOW -> HIGH or HIGH -> LOW; see also the Technical Specifications). A typical response time with maximum resistive load is 70 Ps. See the following diagram for the pin assignments of both interfaces.



Figure 1-2. Pin Assignments of the Input Interface and the Output Interface

1.1.3 Symmetrical 5 V Differential Inputs

The differential inputs are located on the 15-pin sub D socket of the module. The differential inputs interface conforms to the RS422A standard. You can connect 5 V sensors with differential signals to the differential inputs. Maximum input frequency is 58 kHz. The pulse length of the input signals at the 5 V differential inputs (signal "0" (0 V) or "1" (5 V) must be at least 8.6 μ s.

Unwired ("open") 5 V differential inputs are handled by the IP 265 as differential inputs with signal state "1" (5 V).

Figure 1-3 shows you where on the 15-pin sub D socket the signal lines of the 5 V sensors are to be connected. Four pins are reserved on the sub D socket for the two differential inputs. The remaining 10 pins of the 15-pin sub D socket are irrelevant to the use of the counter function (-> see the IP 265 Manual for further information on the pin assignments of the interface).



Figure 1-3. Pin Assignments for the 5 V Differential Inputs



Warning

All pins not used for the standard function counter must remain inactive.

1.1.4 Submodule Receptacle

The submodule with the standard function counter is plugged into the submodule receptacle on the IP 265.

Warning

The memory submodule can only be plugged in or removed when the module is in the POWER OFF state.

1.1.5 **LED Displays**

The frontplate of the IP 265 is equipped with several LEDs:

- 1 red STOP LED
- 1 green RUN LED
- 8 green LEDs for 8 digital 24 V inputs •
- 8 green LEDs for 8 digital 24 V outputs ٠

Either the RUN LED or the STOP LED will light up to indicate the operating state of the IP 265. Faults in the IP 265 are indicated by the STOP LED or by a combination of the RUN and the STOP LED. Different faults are indicated by different flashing signals. See Appendix A for a summary of all the possible status displays of the IP 265 in conjunction with the standard function counter.

2 Installation Guidelines

This section describes how to establish the connections with the programmable controller and the process I/O.

2.1 24 V DC Supply

The IP 265 is a non-floating module. The 24 V DC load current circuits share the same ground with the control circuit of the PLC.

Figure 2-1 shows the simplified connection of the IP 265 to the PLC.



Figure 2-1. Simplified Representation for Non-Floating Connection of the IP 265 to the PLC

Note

When using the IP 265, you must connect the ground of the IP 265 load voltage connector with the CPU ground via an external connection at the central grounding point.

When doing so, please make sure you use a low-resistance connecting cable (cable should be as short as possible).

2.2 Establishing the Connection to the S5-100U Bus

The IP 265 is like an I/O module of the S5-100U system and is snapped onto a bus unit. You must note the following points when assembling and dismantling the module:

- The IP 265 may be plugged in or removed only without load voltage and when the CPU is in the STOP state.
- The memory submodule may be plugged in or removed only when the module and the CPU are in the POWER OFF state.
- The IP 265 can only be snapped onto a bus unit in slots 0 to 7 of the programmable controllers.
- For instructions on assembling and dismantling the module, see the IP 265 Manual or the System Manuals for the S5-100U, S5 90/95U or ET 200.

2.3 Establishing the Connection to the I/O

The following electrical connection must be made depending on your application:

- Connection between 24 V digital inputs of the module and plant sensors
- Connection between 24 V digital outputs of the module and plant actuators
- · Connection between differential inputs of the module and sensors with differential signals
- 24 V power supply

Connecting 24 V digital inputs

The digital inputs of the IP 265 are designed for 24 V DC. The signal lines of the sensors are to be shielded and connected via the 9-pin sub D connector of the IP 265 marked "Input".

Connecting 24 V digital outputs

The digital outputs of the IP 265 are designed for 24 V DC. The signal lines of the digital actuators are to be shielded and connected via the 9-pin sub D socket marked "Output".

Connecting differential inputs

The signal lines of the sensors with 5 V differential signals are connected via the 15-pin sub D socket of the IP 265 marked "Interface". Signal lines of up to 32 m are possible. The signal lines must be shielded Pre-fabricated standard cables can be ordered (see Appendix C). If pre-fabricated cable is not used and if a sensor with 5 V differential signals is to be connected to the IP 265, the 5 V sensor line must also be shielded.

Example: A pulse sensor is to be connected to the IP 265.



Figure 2-2 Connection Example for 24 V Digital Input

Cable connection conditions

To ensure the correct functioning of the IP 265, there are important rules to be observed concerning **wiring** and **shielding**. Since the IP 265 can only be used in conjunction with the S5-100U, S5-90/95U or ET 200, it is assumed that you possess one of the relevant manuals. In the manual you will find details of all cable connection conditions for programmable controllers (PLCs).

The following information refers only to the shielding of the connection cable.

Notes on cable shielding

Both ends of shielded cables should have a good electrical connection to the cabinet's chassis ground. You can effectively suppress interference of all coupled frequencies only if the cables are shielded at both ends. The shield should reach the module and should also be connected to the module!

Note

There can be a compensating current flowing across cables shielded at both ends if there are ground potential fluctuations. You should therefore join the connected components with an additional equipotential bonding cable.

With SIMATIC controllers, the interference current on cable shielding is discharged to ground both via the shielding rail and the equipotential bonding cable. To prevent these discharged currents from becoming a source of interference, ground them on a low-resistance path as follows:

- Tighten the hold-down screws on the cable connectors, modules, and equipotential bonding cables.
- Protect the contact surfaces of equipotential bonding cables against corrosion.

2.4 Further Notes on Configuring and Installing the Module

As the module is usually used as a component in larger systems or plants, the following notes are intended to help you safely integrate the module into its environment.

Notes to be observed for the installation and startup of the module, depending on individual applications:



3 Input and Output Signals

You control the functionality of the counter via the digital inputs of the IP 265 and via data that is transferred to the IP 265 from the CPU via the process image of the outputs (PIQ)

3.1 Counter Pulses at the CU1 and CU2 Input

This input is a direct link with your process. The counter pulses to be processed by the program are applied here.

In the standard function, two inputs per counter channel are provided for the counter pulses:

- One counter input for 24 V signals up to a limit frequency of 10 kHz.
- One high-speed counter input for 5 V differential signals to RS422A with a limit frequency of 58 kHz.

Timing of the counter pulses at the CU1 and CU2 input (5 V differential input)

The following conditions must be observed for the sensor signals:



This results in a minimum pulse time of 17.2 μ s. The maximum input frequency is then 58 kHz. The mark/space ratio is variable. However, the minimum time limits must not be violated.

3.2 Signals that have an Influence on Counting

Counting is influenced by additional signals over hardware inputs or paramters in the PIQ.

3.2.1 Resetting an Output (RSQ)

There is an RSQ signal for every counter channel. The assigned ouptut A can be reset with the RSQ signal. The input responds to the rising edge of the RSQ signal. The counter status is not influenced by setting RSQ.

3.2.2 Resetting a Counter Channel (RSC)

There is an RSC signal for each counter channel. The rising edge of the signal sets the counter status of the assigned channel as follows:

- to zero in the case up counting (normal counter function)
- to the specified setpoint in the case of down counting (periodic counter function and cascading function).

In addition, down counting resets any output which has been set.

3.2.3 GATE Signal (GATE)

You can interrupt an active count with the active GATE signal.

The signal GATE = "1" stops the count despite pending counter pulses. The assigned output is switched off simultaneously if it was switched on.

The state remains until the GATE signal is set to "0" again.

With the value GATE = "0", the output is returned to the old state and the count is continued simultaneously.

The GATE signal is subordinate to the RSQ and RSC signals, i.e. the RSQ and RSC signals remain functional even if the count is stopped.

3.3 Counter Output

Each counter channel of the standard function counter is assigned an output and the corresponding negated output of the IP 265. Signalling of a set output via a bit in the PIQ runs parallel to this. Outputs are set when the count passes zero only in the down counting functions (PCF (periodic counter function) and CAF (cascade function)).

Outputs can be reset by the rising edge of the following:

- RSQ signal
- RSC signal

3.4 Location of the Signals in the Process I/O Images

The location of the inputs and outputs on the module is described in Section 2. The locations in the process I/O image are as follows:



Only the control signals and the output signal of channel 1 are decisive for the cascade function. Output Q2 is always "0" in the cascade function.

3.5 ORing and Evaluating Signals

There are two signal inputs for different signals of the standard function counter:

- Hardware inputs
- PIQ data

These "inputs" are ORed with each other internally. They are always active simultaneously and can be driven independently of each other.

This means, for example:

- The CU counter pulses can be routed either via a 24 V digital input or a 5 V digital output.
- The signal for resetting the counter channel (RSC) can be given either via a 24 V digital input or via a bit in the PIQ of the CPU.

The outputs are active at the hardware output and in a bit in the PII simultaneously. The negated output signal has no equivalent in the PII.

0	24 V		БІО	24 V		Signal E	valuation
Signals	DI	5 V DI	PIQ	DQ	PII	Edge-Triggered	Value-Triggered
CD	•	•				Rising Edge	
RSQ	•		•			Rising Edge	
RSC	•		•			Rising Edge	
GATE	•		•				"1"
Q				•	•		
Q\				•			

Table 3-1 ORing the Interfaces of the Standard Counter Function

4 The Counter Functions

The program offers you three different function modes for your applications. You can change these modes according to your needs via the STEP 5 program. The functions are called:

- Normal counter function NCF
- Periodic counter function PCF
- Cascade function CAF

Two independent 16-bit counters can be used in the NCF and PCF.

A 32-bit counter is available for the CAF.

Normal counter function NCF

The normal counter function is a simple 16-bit up counter. Each counter pulse at the CU input increments the counter status by 1. When the maximum count has been reached, counting continues from zero.

No outputs are set in this function; the outputs are generally reset.

Periodic counter function PCF

The periodic counter function is a 16-bit down counter. At the starting point of the periodic counter function, the counter is set to a specified setpoint. Each counter pulse at the CU input decrements the count by 1 starting from the setpoint. If the count reaches 0, the assigned output is set and the count is reset to the setpoint.

A set output can be reset via the RSQ or RSC signals.

Cascade function CAF

The cascade function is a down counter like the periodic counter function but with a data width of 32 bits. It operates in the same way as the periodic counter function.

4.1 Selecting the Counter Function Mode

There are three bits available in the process image of the outputs (PIQ) for selecting the mode. You use these bits to set the relevant mode. Both channels can be switched to the "normal counter function" mode or the "periodic counter function" mode independently of one another.

Note	
The function modes can only be set via the to the IP 265.	STEP 5 program and output via the PIQ

Location of the bits in the function mode byte:



Note	
Setting and transferring the bits to the IP 265 does not yet start the new function.	

Transfer of the bits by the IP 265 and starting of the new function mode are described in the next section.

4.2 Transferring the Set Function Mode Using the IP 265

Switching from one function mode to another can be divided into the following steps:

- 1. Specification of the function mode using the CASC, CF1 and CF2 control bits.
- 2. Transfer and start of the new function with the RSC1 and RSC2 control bit.

4.2.1 Switching from Two-Channel Mode to Cascade Mode

If you want to switch the standard counter program from two-channel mode (PCF, NCF) to single-channel mode (CAF), follow these steps:

- Set the CASC bit to "1".
- Set **both** reset signals RSC1 and RSC2 to "1".

Note

In order to switch on the cascade function, both reset signals RSC1 and RSC2 must be set simultaneously. This is only possible if both signals are transferred to the IP 265 over the PIQ in the same data cycle.

The IP 265 detects both rising edges and switches the standard function to the cascade function.

Note

When the cascade function is switched on, only the data and control bits of channel 1 are active. Changes to channel 2 have no effect.

4.2.2 Switching from the Cascade Function to Two-Channel Mode

You switch the standard counter program from single-channel mode (cascade function) to twochannel mode (PCF, NCF) as follows:

- Set the CASC bit to "0"
- Set the RSC bit to "1".

This resets both channels. The new function in which you then work follows the assignment of bits CF1 and CF2

	CF1 = 0	CF1 = 1
CF2 = 0	Channel 1 in PCF Channel 2 in PCF	Channel 1 in NCF Channel 2 in PCF
CF2 = 1	Channel 1 in PCF Channel 2 in NCF	Channel 1 in NCF Channel 2 in NCF

4.3 Counter Statuses and Signal Flow in the Three Function Modes

The interplay of the individual signals and the sequence of a count process are essential to an understanding of the functions. For this reason the signal sequence is described briefly in the following two subsections.

4.3.1 The Normal Counter Function

The normal counter function is a 16-bit up counter which works without setpoints and has no direct access to the IP output.

The following example should make the signal sequence clear. Before the start of the function, the counter was set to the PCF function on both channels. The output of channel 1 was set.



Figure 4-1. Pulse Diagram for Channel 1

"Normal counter function" is selected for channel 1 with CF1 = 1. The rising edge of the RSC1 signal sets the counter to the start value "0" for NCF

Output A is switched off when you switch to the normal counter function. This output is not set in the normal counter function.

Reset signals via input RSQ remain without effect for this reason.

The **GATE signal** is transparent throughout, i.e. the reset signals for the counter can still be switched even when the GATE signals are active.

However, pending counter pulses do not change the current counter status.

The Periodic Counter Function 4.3.2

The periodic counter function is a 16-bit wide down counter.

The counter in Section 4.3.1 is to be switched to the "periodic counter function". For this purpose, control bit CF1 receives a new assignment during the current count .



Figure 4-2. Pulse Diagram for Channel 1 (Down Counter)

Principle of operation

- 1. Specifying the PCF function via the CF1 bit does not affect the current count .
- 2. The rising edge of RSC1 has the following effects.
 - Implements the new function mode
 - Sets the counter to the setpoint
 - Starts the count.
- 3. The active GATE signal 3 interrupts the count despite further counter pulses. If the assigned output is switched on, it will be switched off for the duration of the GATE signal .
- 4. The count is continued when GATE = "0".
 - · The counter continues to count in the case of maintained status
 - The output is reset to the "old" status before activation of the GATE signal
- 5. When "0" is reached
 - · The counter is set to the setpoint
 - The relevant output is switched on .
- 6. The RSQ reset input switches the output off .
- 7. The RSQ reset signal is insignificant if the relevant output is not set .

4.3.3 The Cascade Function

The cascade function is a 32--bit wide down counter. Its functionality is no different to the periodic counter function.

In the following timing diagram, the periodic counter function has been selected as the starting configuration for both channels.



* Counter pulses on channel 2 have no effect during operation of the CASC function.

Figure 4-3. Pulse Diagram for Cascade Function (Down Counter)

Principle of operation

- 1. If the CASC bit is set to "1", the settings of bits CF1 and CF2 have no significance .
- 2. The counter is prepared for the cascade function by setting the CASC bit to "1" .
- 3. The cascade function is switched on with the rising edge of RSC1 and RSC2 . The specified setpoint is loaded simultaneously. From this point, all channel 2 signals are meaningless and without effect.
- 4. After the CASC bit has been reset and a rising edge has been detected at input RSC1, the standard counter function is set back to two-channel mode. The operating modes of both channels follow the status of the CF1 and CF2 bits at the point of changeover.
- 5. A set output is reset by the rising edges of the RSC1 and RSC2 signals .
- 6. The new setpoint (1000) is loaded into channel1 in the case of a rising edges of singal RSC1.

4.4 Value Range for Setpoints and Counter Values

The value range depends on the selected function mode. The following table gives you an overview of the formats used:

Function Mode	Data Width	Counter Range
Normal counter function (NCF)	2 byte 6 16 bit	Start value 0 End value max. 65535
Periodic counter function (PCF)	2 byte 6 16 bit	Start value corresponding to the setpoint specified max.65535 End value 0*
Cascade function (CAF)	4 byte 6 32 bit	Start value corresponding to the setpoint specified max.4294967295 End value 0*

* The current setpoint is transferred as soon as the end value "0" is reached. This means that evaluation for "0" is only possible over the corresponding counter output (Q1, Q2).

All counter values and specified setpoints are represented as numbers without sign.

4.5 Loading the Setpoints

A setpoint need not be specified in NCF.

A setpoint > 0 must be specified for operating the counter in the "periodic counter function" and in the "cascade function".

Both functions count down to zero from the specified setpoint. When "0" is reached, the assigned output is switched on and the setpoint is set simultaneously.

Note

When changing from counter status "1" to counter status "0", the counter is set to the predefined setpoint.

If no setpoint is specified, zero is taken as default. Counting is then not possible in PCF and CAF and the outputs remain reset.

Specifying and Implementing a Setpoint 4.5.1

For the purpose of specifying a setpoint, you must assign the parameter area in the PIQ of the CPU according to the counter function.

The location of the setpoint values and the counter values in the process I/O area depends on the function modes set.

The following overview shows you the location of the setpoint values and counter values in the PIQ and PII for the 3 function modes.

Normal counter function

Byte number	Meaning PIQ		Meaning PII	
2	insignificant		High byte	Counter value 1
3	insignificant		Low byte	
4	insignificant		High byte	Counter value 2
5	5 insignificant		Low byte	

Periodic counter function

Byte number	Meaning PIQ		Meaning PII	
2	High byte	Setpoint 1	High byte	Counter value
3	Low byte		Low byte	
4	High byte	Setpoint 2	High byte	Counter value
5	Low byte		Low byte	

1

2

Cascade function

Byte number	Meaning PIQ		Meaning PII	
2	High byte	Setpoint	High byte	Counter value
3	Low byte	High word	Low byte	High word
4	High byte	Setpoint	High byte	Counter value
5	Low byte	Low word	Low byte	Low word

New setpoints can be specified at any time via the relevant PIQ area of the counter. However, the setpoint is only transferred with the rising edge of RSC or when the counter passes zero.

Note

If the counter program detects a rising edge at the RSC input of the relevant channel, a setpoint must be specified otherwise the counter will enter a zero loop (start value "0", end value "0"). The assigned output will never be set.

When specifying a setpoint, enter the value in KH format in the relevant output words in the PIQ.

5 Addressing

Addressing the IP 265

The IP 265 can be used in slots 0 to 7 of the S5-100U. For each slot, there are eight bytes reserved in the process image of the outputs (PIQ) and eight bytes in the process image of the inputs (PII). Data is interchanged between the CPU and the IP 265 via all eight bytes of the PII and the PIQ.

PS CPU	0	1	2	3	4	Slot:	s 6	7	8
Analog	64	72	80	88	96	103	112	120	Cannot be used
addresses	to	to	to	to	to	to	to	to	from slot 8 on
	71	79	87	95	103	111	119	127	

The permissible address range is 64 to 127. The IP 265 is referenced with bytewise or wordwise load and transfer operations, in the same way as analog input modules or analog output modules.



The IP 265 exchanges data with the CPU of the programmable controller over the S5-100 bus.

The addresses under which you must reference the PII or PIQ depend on the slot into which you have plugged your module. For this reason, only the address offset for the start address of the slot in each case has been given in the following explanation of the individual bytes.

You have plugged your IP 265 into slot 2 of the programmable controller. The start Example:

address is 80.

"Byte 6" in the following refers to the offset of address 80. You therefore reference

byte (80 + 6). The load and transfer operations programmed by you must therefore refer to byte 86.

- L IB 86
- T QB 86

Meaning of the bytes of a slot (example: slot 1)

The following table gives you an overview of the assignment of the process I/O images. The IP 265 has been inserted into slot 1 in the example. The start address of the address area is therefore 72. In addition, the table contains cross-references to the sections in which the individual bytes are described.

Byte number	Byte address	Meaning PIQ	Meaning PII
0	72	Control word IP 265	Status word IP 265
1	73	Section 6	Appendix A
2	74		
3	75	Setpoint range	Counter range
4	76	Section 4.5	Section 4.5
5	77		
6	78	Signal byte, bit 0 5	Output byte
		Section 3.4	Section 3.4
7	79	Function mode byte bit 4 6 Section 4.1	Not insignificant

Loading and Starting the Standard Function 6

The IP 265 must be set to POWER OFF when the submodule is being inserted.

- Switch off the programmable controller
- Slide the submodule into the receptacle until it engages. Then switch the programmable controller on again.

The IP 265 now loads the PLC program from the submodule. The IP 265 indicates that loading is in progress by flashing the STOP LED on the frontplate of the module.Loading is completed after approximately 3 seconds.

The STOP LED now remains lit.

Status of the IP 265 after loading from the submodule

After the submodule program has been loaded, the IP 265 is in the STOP state.

- Execute the following steps to start the IP 265:
- If the CPU is at STOP, switch it to RUN.
- Now switch the IP 265 to RUN also via the IP 265 control word.

Note

The RUN bit must always be set during counting. Communication between the CPU and the IP 265 is not possible with RUN = "0".

If the CPU goes to STOP, the IP 265 also goes to STOP. The counter function is then not processed. After a renewed STOP RUN transition, the counter function must be reset.

Structure of the control word (byte 0, byte 1)



The RUN LED lights up after transfer of the RUN command. The IP 265 with the standard function counter is in operation.

A Diagnostics and Error Messages

The actual operating state can be diagnosed and the error messages can be monitored over the status word.





The group error bit is set in the case of every error.

A.2 LED Displays

Operating states and fault states can be detected via the STOP and RUN LEDs as well as by using the diagnostics possibilities of the status word:

STOP LED	RUN LED	Status	Diagnosis	
Constant light		STOP	Desired STOP	
Flashing light		STOP	Group error (for every error)	
Flashing light	Constant light	RUN	Short-circuit at the output	
	Constant light	RUN	Status	
Rapid flashing		STOP	Load from the submodule	

Technical Specifications Β

Module		
Permissible ambient temperature		
- vertical configuration		0 +40 °C
Current consumption from + 9 V (CPU)		<175 mA
Insulation rating		to VDE 0160
Signal status display		Only for 24 V inputs and 24 V outputs (green LEDs)
Status indicators		for STOP (red LED) for RUN (green LED)
Memory submodule		EPROM/EEPROM
Adress code for ET 200 (slow mode only)		223
Weight	approx.	300 g
Digital 24 V inputs		9-pin sub D connector
Number of inputs		8
Galvanic isolation		no
Status indication		yes, on 5 V side
Input voltage L+ - nominal value - for "0" signal - for "1" signal		24 V DC 0 5 V 11 30 V (IEC 65 A)
Input voltage for "1" signal	typ.	6.5 mA (IEC 65A)
Connection of 2-wire BERO		possible (quiescent current 1.5 mA)
Input frequency	max.	10 kHz
Cable length (shielded)	max.	100 m/325 ft.
Input circuit delay		
- rising edge - falling edge	typ. typ	15 μs 10 μs
5-V differential inputs	-76.	15-pin sub D HD socket
Number and type of input signals - for standard function counter		2 differential signals to RS 422 AA-N, BB-N
Counter frequency	max.	58 kHz
Pulse length		
- Low level	min.	8.6 μs
- High level	min.	8.6 µs
Cable length (shielded)	max.	32 m/105 ft.

Digital 24-V Outputs		9-pin sub D socket			
Number of outputs		8; in the standard function counter 2			
Galvanic isolation		no			
Status indicator		on 5-V side	on 5-V side		
Short-circuit protection		yes, electronically clocked			
Load voltage L + - nominal value - permissible range		24 V DC 20 30 V			
Output current at "1" signal		0.5 A at 60°C			
Permissible total current of the outputs		2 A at 60°C			
Output frequency in the case of	max. max. max.	1 kHz 2 kHz 4 kHz	at at at	15 mA load* 50 mA load* 500 mA load*	
Cable length	max.	100 m/325	ft.		
Lamp loadmax.	max.	2 W			
Residual current at "0" signal	max.	1 mA			
Voltage drop with "1" signal max.		1 V			
Voltage induced on circuit interruption limited to		- 15 V			
Output circuit delay - rising edge - falling edge	typ.	10 µs			
dependent on resistive load	typ. typ. typ.	150 μs 90 μs 70 μs	at at at	15 mA load* 50 mA load* 500 mA load*	

Peak value (not an r. m. s specification)

Note

The IP 265 can only be used in the S5-90U, S5-95U, S5-100U (CPU 100 and 102 from operating system version Z0 6, CPU 103) and the ET 200 system from version Z02 (from -8MB11) of the IM 318-B.

С **Ordering Numbers**

Connecting cables for position encoders

The following prefabricated connecting cables are available for connecting pulse sensors to the 5-V differential inputs of the IP 265 (RS 422A):

•	706 connecting	g cable for SIEMENS position encoders 6FC9320	
	Length	5m/16.4 ft	6ES5 706-7BF01
	Length	16m/52.5 ft	6ES5 706-7CB61
	Length	32m/105 ft	6ES5 706-7CD21
•	706 connecting	g cable with open ends	
	Length	5m/16.4 ft	6ES5 706-8BF01
	Length	16m/52.5 ft	6ES5 706-8CB61
	Length	32m/105 ft	6ES5 706-8CD21
Sta	ndard functior	n counter	
Star	ndard function of	counter (submodule and description)	6ES5 840-4SH01

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Siemens AG	Sender (Please fill out)
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	Company/Department
D-92209 Amberg	
Fed. Rep. of Germany	 Address
Suggestions: Corrections:	
Standard Function Counter	Telephone
Edition 2	

Have you found any typographical errors while reading this manual? Please use this form to tell us about them.

We would also welcome any ideas and suggestions you may have.